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TOTAL DOSE HARDNESS ASSURANCE. VOLUME II. VERIFICATION TEST RES-ETC(U)

FEB 80 R L PEASE, P A YOUNG

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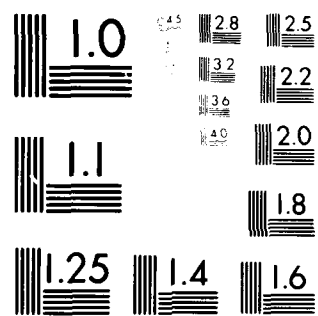
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**PHASE I COMPLETION REPORT  
TOTAL DOSE HARDNESS ASSURANCE**

Volume II: Verification Test Results

BDM Corporation  
Albuquerque, NM 87106

February 1980

Final Report

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This research was sponsored by the Defense Nuclear Agency under Subtask Z99QAXTD072, Work Unit 14, Hardness Assurance Techniques for LSI Devices.

Prepared for

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This final report was prepared by BDM Corporation, Albuquerque, New Mexico, under Contract F29601-78-C-0022, Job Order 88091133 with the Air Force Weapons Laboratory, Kirtland Air Force Base, New Mexico. Mr. Roe J. Maier (NTMP) was the Laboratory Project Officer-in-Charge.

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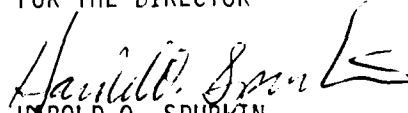


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| REPORT DOCUMENTATION PAGE  |  | READ INSTRUCTIONS<br>BEFORE COMPLETING FORM   |  |
|--|--|---|--|
| 1. REPORT NUMBER<br>AFWV-TR-79-53, Vol. II of II   |  | 2. GOVT ACCESSION NO.<br>AD-A085013   |  |
| 3. TITLE (and Subtitle)<br>PHASE I COMPLETION REPORT<br>TOTAL DOSE HARDNESS ASSURANCE.<br>Volume II, Verification Test Results.  |  | 4. TYPE OF REPORT & PERIOD COVERED<br>Final Report.   |  |
| 5. AUTHOR(s)<br>R. L. Pease<br>P. A. Young   |  | 6. PERFORMING ORG. REPORT NUMBER<br>BDM/TAC-78-764-TR-R1-VOL-2  |  |
| 7. PERFORMING ORGANIZATION NAME AND ADDRESS<br>BDM Corporation<br>Albuquerque, New Mexico 87106  |  | 8. CONTRACT OR GRANT NUMBER<br>F29601-78-C-0022   |  |
| 9. CONTROLLING OFFICE NAME AND ADDRESS<br>Air Force Weapons Laboratory (NTMP)<br>Kirtland Air Force Base, NM 87117   |  | 10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS<br>64711F<br>88091133   |  |
| 11. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)<br>Ronald L. Pease<br>Phil A. Young  |  | 12. REPORT DATE<br>Feb 1980   |  |
| 13. DISTRIBUTION STATEMENT (of this Report)<br>Approved for public release; distribution unlimited   |  | 13. NUMBER OF PAGES<br>92   |  |
| 14. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)   |  | 14. SECURITY CLASS. (of this report)<br>UNCLASSIFIED  |  |
| 15. SUPPLEMENTARY NOTES<br>This research was sponsored by the Defense Nuclear Agency under Subtask Z99QAXTD072, Work Unit 14, Hardness Assurance Techniques for LSI Devices.   |  | 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE<br>1.2001, Z99QAXT   |  |
| 16. KEY WORDS (Continue on reverse side if necessary and identify by block number)<br>Ionizing Radiation<br>Silicon Dioxide/Silicon Interface<br>Radiation Effects<br>Semiconductors   |  | 16. KEY WORDS (Continue on reverse side if necessary and identify by block number)<br>Bipolar Devices<br>MOS Devices<br>Hole Trapping<br>Interface Defects<br>Radiation Simulation<br>Hole Injection<br>Radiation Testing<br>Semiconductor Models<br>Hardness Assurance |  |
| 17. ABSTRACT (Continue on reverse side if necessary and identify by block number)<br>This report covers the first phase of a three phase program to develop hardness assurance techniques for the total ionizing radiation dose environment for bipolar and MOS semiconductor devices. Phase I consists of identifying and verifying potentially useful techniques. The report is presented in two volumes. Volume one discusses all of the potential hardness assurance techniques that were identified and whether or not they are sufficiently verified in previous studies. In addition, new techniques are proposed based on models of radiation-induced hole trapping and interface state generation. (over) |  |   |  |

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Each technique identified or proposed is discussed in terms of its implementation, cost effectiveness, and acceptability. Recommendations are made for each technique to: a. reject for this program, b. verify its usefulness with further testing or, c. accept as useful and include in the evaluation phase. The techniques investigated fall into five major categories: 1. pre-irradiation device electrical tests, 2. preirradiation tests on special test devices or wafers, 3. process or design controls, 4. radiation simulation tests, and 5. radiation tests. Over 20 techniques were identified and 9 were selected for further studies.

Volume II is a summary of the test results of the verification tests performed on commercial semiconductor devices. These verification tests were performed either to supplement the limited available data for a potentially useful technique or to generate original data on previously unexamined techniques. The correlation coefficient was determined between the screening parameter and the total dose induced change in device electrical parameters on groups of 5-25 devices of a given type. No high degree of correlation was observed for any of the techniques investigated with the exception of irradiate and anneal on MOS devices.

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## SECTION I

### INTRODUCTION

The specific objectives of phase I of the Total Dose Hardness Assurance (HA) Program are to

- (1) Identify all possible total dose HA techniques using literature, personal contacts and techniques conceived from models of basic mechanisms.
- (2) Determine the effectiveness and practicability of each of the techniques using existing data, experience and analysis.
- (3) Verify by experiment the effectiveness of those techniques for which an insufficient amount of data exists to reasonably establish their usefulness.

A complete discussion of the total dose HA techniques that have been identified in this program has been presented in volume I along with discussion of their effectiveness and practicality in terms of existing data, basic mechanisms models and analysis.

This report, volume II, covers the results of experiments which were performed on discrete devices in order to verify those techniques for which insufficient test data existed. The techniques which were experimentally investigated included: (1) techniques which appear promising but which had not been verified to a sufficient extent, (2) techniques which had been experimentally researched but had not been applied directly as a hardness assurance method, and (3) techniques which had been conceived from models of hole trapping or interface state generation and thus had not previously been experimentally investigated.

Because of the limitations imposed on the verification testing during phase I, several techniques which required verification testing were not investigated. This was due either to the unavailability of the appropriate test devices, e.g., gated bipolar transistors or gated diodes, or the requirement for in-process testing such as would be done on test wafers during processing. Since several of the techniques that require

some verification testing were not included in the phase I verification test program, it was decided that the verification testing would be done during the initial part of the phase II evaluation program. Therefore, this report does not address all of the verification testing that will be performed on the program but only that portion performed on "off-the-shelf" discrete MOS or bipolar components.

The basic approach to the phase I verification testing was to measure the correlation coefficient between the screening parameter and the radiation hardness of a small number of samples of a commercial device type. The number of samples ranged from 10 to 25. All irradiations were done under bias on a Co<sup>60</sup> source at a fixed dose level.

A full description of the various techniques that were investigated in the phase I verification tests is given in volume I of the phase I completion report. However, a brief summary of each technique is included herein. Each section of the report, which addresses a different technique, contains, in addition to a brief description and rationale, a discussion of the approach, the samples used for the testing, the electrical tests performed, the irradiation tests, data analysis, results and suggestions for improving the technique, if applicable.

## SECTION II

### AVALANCHE HOLE INJECTION

#### 1. OBJECTIVE

The objective of this experiment is to determine if a correlation exists between parameter changes resulting from avalanche hole injection and the damage produced by total ionizing dose.

#### 2. RATIONALE

Hole trapping parameters of the oxide found by avalanching an underlying p-n junction have been investigated by Verwey ( refs. 1, 2). Avalanching a p-n junction under an oxide produces holes sufficiently energetic to enter into the oxide, where they either escape to the negatively biased gate electrode or are trapped within the oxide. The altered electrical behavior of the stressed device caused by trapped positive charge yields the data required to calculate oxide trapping parameters.

An oxide with relatively few hole traps would be expected to be less susceptible to the effects of total ionizing dose. Therefore, the total number of hole traps ( $N_t$ ), as determined by the avalanche injection technique, should act as a screen for parts which would show an unacceptable degradation in a total dose environment.

The original technique developed by Verwey assumes a field dependent hole current through the oxide. To determine  $N_t$ , the concentration of hole trapping centers times the capture cross section; transient picoamp hole current measurements must be made at several oxide electric field values. Complex data reduction is required, including numerical integration of measured data. Assumptions required include the diffusion length of hot holes, the interface area of the avalanching region, and uniform injection over the avalanche area.

To avoid some of the difficulties of the Verwey technique, a new technique was developed by BDM. The experimental procedure utilized is illustrated schematically in Figure 1. The p-n junction is avalanched by a fixed amount of current and the breakdown voltage immediately noted. Energetic holes attracted to the negative gate bias enter the oxide, where some are trapped. The trapped positive charge in the oxide will alter the surface potential and causes the breakdown voltage to increase. The gate bias is then made more negative to restore the initial breakdown voltage and surface potential. Under constant surface potential, the growth of the trapped oxide charge will be described as:

$$Q(t) = qN_t (1 - \exp(-t/T_c)) \quad (\text{Eq. 1})$$

where  $N_t$  is the number of oxide traps,  $t$  is time, and  $T_c$  is the capture time constant. By letting time approach infinity (allowing the system to approach a static condition),  $Q(t) = qN_t$  as nearly all oxide traps are filled in the region of avalanche injection. The total number of oxide traps can be calculated as:

$$N_t = \frac{\Delta V_G \epsilon_{ox} \epsilon_o}{q X} \quad (\text{Eq. 2})$$

where  $\Delta V_G$  is the range over which the gate voltage was adjusted and  $X$  is the distance from the gate to the centroid of charge. Bakowski et al. (ref. 3) have found the traps to have characteristic distances from the semiconductor of 150-200 Å for dry oxides and about 400 Å for wet oxides. If the distance from the semiconductor to the charge centroid can be assumed to be much less than the oxide thickness, equation (2) can be approximated by:

$$N_t = \frac{\Delta V_G \epsilon_{ox} \epsilon_o}{q d_{ox}} \quad (\text{Eq. 3})$$

where  $d_{ox}$  is the oxide thickness.

METHOD OF DETERMINING  
TOTAL OXIDE HOLE TRAP DENSITY

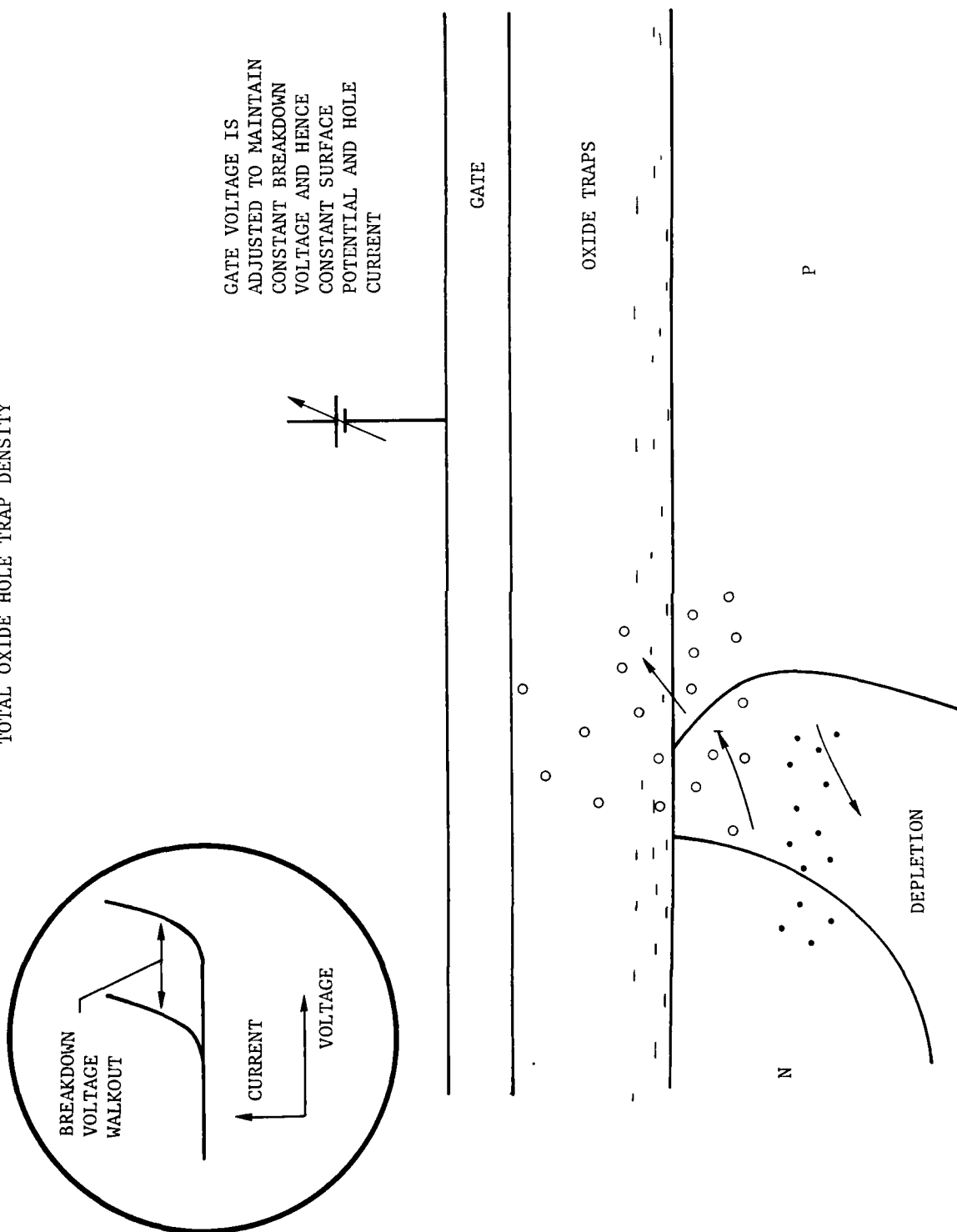


Figure 1. Method of Determining Total Oxide Hole Trap Density

Also investigated was the magnitude of the breakdown voltage increase or breakdown voltage "walkout" produced by a fixed negative gate voltage.  $W V_t$  for this condition can be obtained by reducing the p-n junction voltage to the original breakdown voltage and then decreasing the gate voltage until avalanche is initiated.

### 3. SAMPLES

The experimental test devices chosen were RCA 40468A MOSFETs. The 40468A is a large area N-channel depletion mode DMOS device with no gate protection. It is packaged in a TO-72 metal can. Figure 2a is a photomicrograph of the device and Figure 2b is a cross section and doping profile of the DMOS structure. Table 1 lists some of the important electrical characteristics of the device. A total of ten devices were used for the correlation studies.

### 4. ELECTRICAL TESTS

The threshold voltages of the test devices were determined by plotting drain current as a function of gate voltage with a drain voltage of 50mV. Threshold voltage was obtained by extrapolating along the line segment where transconductance is a maximum to the  $I_D = 0$  line.

### 4. STRESS TESTS

The avalanche injection stress was performed on a Tektronix 577 curve tracer in the sweep mode. The breakdown voltage "walkout" or increase which can occur quite rapidly upon avalanche can be precisely monitored with the storage feature.

The source lead was stressed with a current of 100 mA with the drain floating and the substrate grounded. The initial gate bias was -10V. The source was stressed for 5 minutes. Avalanche of the drain would be impractical since the junction formed by the drain diffusion is not gated as shown in Figure 2.

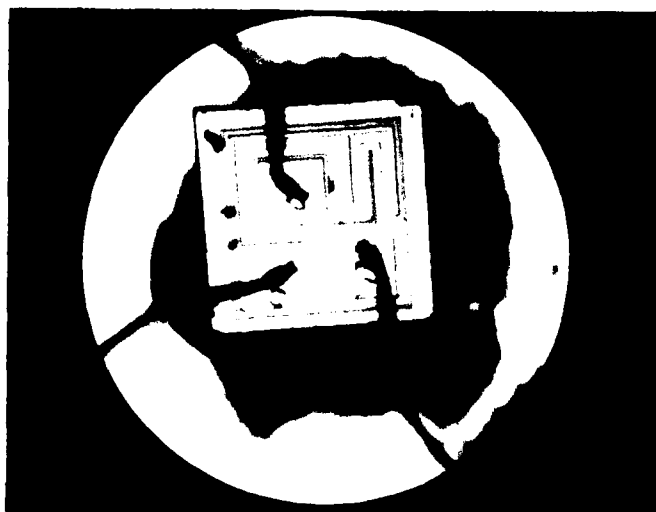


Figure 2a. Photomicrograph of the RCA 40468A (X36)

After the five minute stress, the change in gate voltage, ( $\Delta V_G$ ), was recorded. The gate voltage throughout the stress was constantly adjusted in a manner which kept the breakdown voltage of the source at a constant value.

In the second experiment, the source lead of undamaged samples was again stressed at 100  $\mu$ A with the drain open and the substrate grounded. This time, however, the gate voltage was not adjusted but left at -10V. Stress time was 1 minute.

Under these conditions, the breakdown voltage of the source was allowed to "walkout" or increase. After stress, the gate voltage was reduced to zero volts and the voltage applied to the source was reduced to a value equal to the initial source breakdown voltage. The gate voltage was then increased slowly until breakdown was just initiated. This value was defined as the "gate recovery voltage".

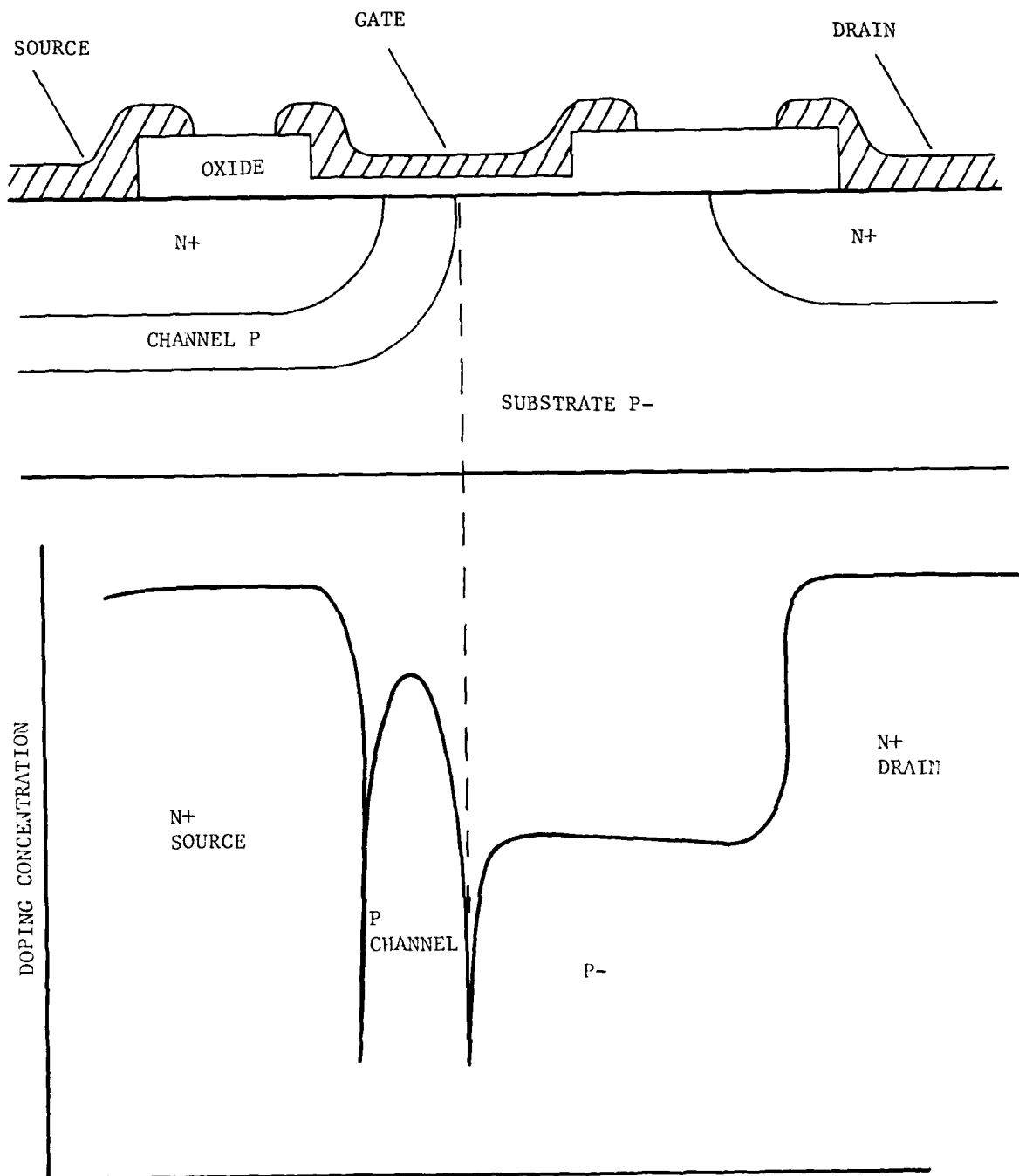


Figure 2b. Cross Section and Doping Profile of DMOS Transistor

TABLE 1. ELECTRICAL CHARACTERISTICS OF THE RCA 40468A

| Characteristics  | Symbols              | TEST CONDITIONS |                            |                       |        |      |      |       |
|--|----------------------|-----------------|----------------------------|-----------------------|--------|------|------|-------|
|  |                      | Frequency       | DC Drain-to Source Voltage | DC Drain Current      | Limits |      |      | Units |
|  |                      | f<br>MHz        | V <sub>DS</sub><br>V       | I <sub>D</sub><br>mA  | Min.   | Typ. | Max. |       |
| Drain-to-Source Cutoff Current   | I <sub>D</sub> (off) | -               | 12                         | V <sub>GS</sub> = 8V  | -      | -    | 100  | μA    |
| Gate Leakage Current   | I <sub>GSS</sub>     | -               | 0                          | V <sub>GS</sub> = -8V | -      | -    | 1    | nA    |
|  |                      | -               | 0                          | V <sub>GS</sub> = +1V | -      | -    | 1    | nA    |
| Zero-Bias Drain Current  | I <sub>DSS</sub>     | -               | 15                         | V <sub>GS</sub> = 0   | 5      | 15   | 30   | mA    |
| Small-Signal, Short-Circuit Forward Transconductance                     | g <sub>fs</sub>      | 1 KHz           | 15                         | 5                     | -      | 7500 | -    | μmho  |
| Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate) | C <sub>rss</sub>     | 1               | 15                         | 5                     | -      | 0.25 | 0.35 | pF    |
| Input Capacitance  | C <sub>iss</sub>     | 1               | 15                         | 5                     | -      | 5.5  | -    | pF    |
| Maximum Available Power Gain   | MAG                  | 100             | 15                         | 5                     | -      | 26   | -    | dB    |

## 6. IRRADIATION

The devices were irradiated by exposure to the AFWL 5 kilocurie  $\text{CO}^{60}$  gamma ray source. The total dose received was  $5 \times 10^5$  Rad (Si). A positive 1 volt bias was applied to the gate during the irradiation and all other leads were grounded.

## 7. RESULTS

Figure 3 is a plot of  $\Delta V_G$  (directly proportional to  $N_t$ ) as a function of the change in threshold voltage. The negative slope of the least squares fit line and poor correlation coefficient indicates that knowledge of  $N_t$  will give no indication of the magnitude of threshold voltage shift at  $5 \times 10^5$  Rad (Si).

The disappointing results can be explained by the fact that threshold voltage shift is also a function of interface state generation. Consider the "growth curves" proposed by Freeman and Holmes-Siedle (ref. 4) in Figure 4. At low doses the threshold voltage shift caused by hole capture produces a linear change in the log of  $\Delta V_t$  with respect to Log of dose. At higher doses, the hole trapping saturates and the shift produced by surface states become dominant in a nonlinear manner.

The unhardened samples tested were irradiated to  $5 \times 10^5$  Rad (Si) which may be well into the trap dominated nonlinear region. If these devices were irradiated in the nonlinear region, no correlation between  $N_t$  and  $\Delta V_t$  could be expected.

A further study of the work of Freeman and Holmes-Siedle indicates that avalanche hole injection may be of great use in total dose hardness assurance. Two "engineering growth curves" shown in Figures 5 and 6 are suggested as useful "for making predictions of the lifetime of MOS circuits exposed to radiation in space or laboratory environments."

The curves of Figure 5 predict that the maximum threshold shift under a negative gate bias is the gate voltage applied. This effect should be seen in the second experiment and will act as a check on the

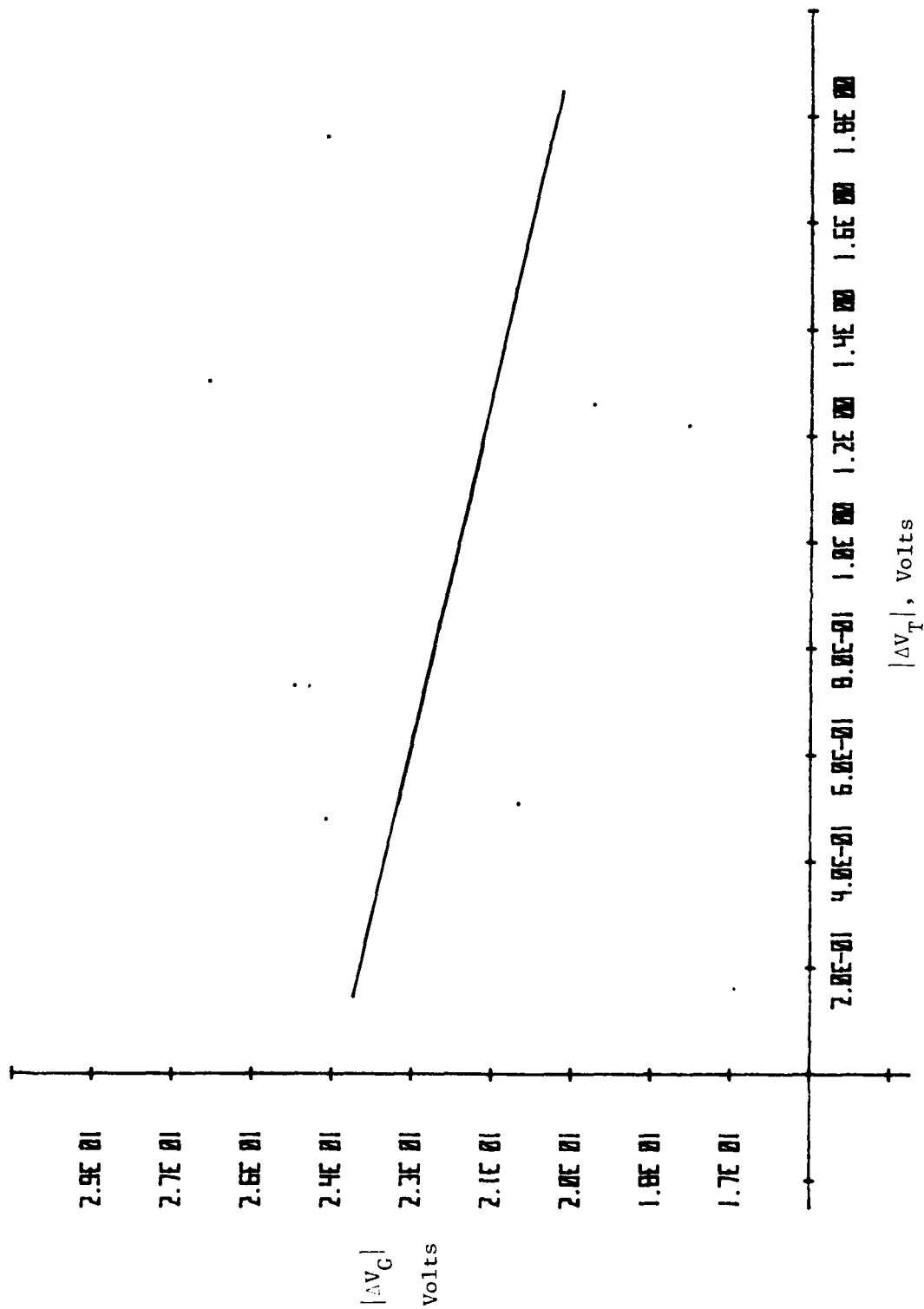


Figure 3. Change in the Gate Voltage Required to Maintain Constant Surface Potential as a Function of the Radiation Induced Threshold Voltage.  $R = 0.3555 \pm 0.31$ .

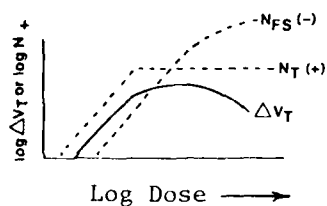


Figure 4. Typical Damage Growth Curve

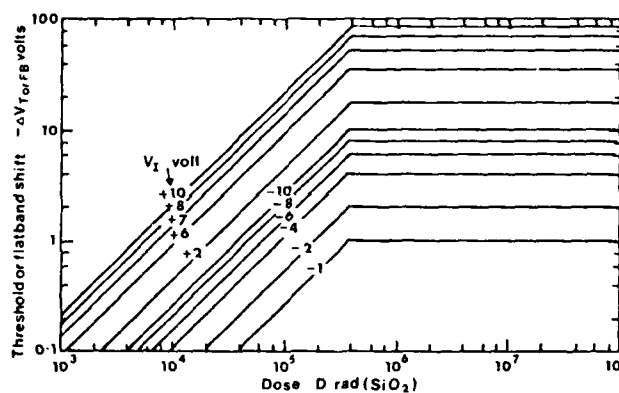


Figure 5. A set of growth curves, suitable for use by design engineers, based on a simple charge sheet buildup model. Saturation shown here is due to oxide field vanishing.

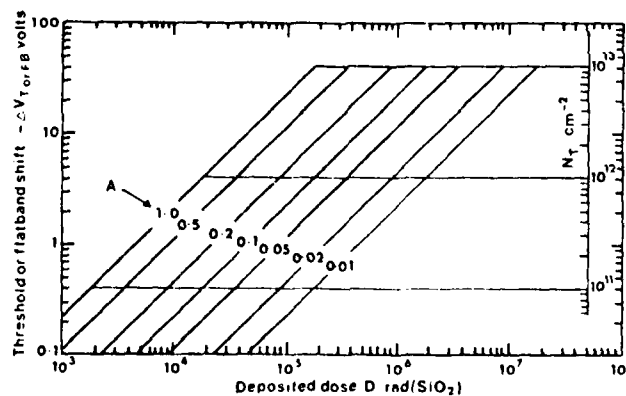


Figure 6. A set of growth curves, suitable for use by design engineers, based on a simple charge sheet buildup model. Saturation is due to trap filling.

validity of the avalanche hole injection technique. Assuming trap saturation did not occur, the "gate recovery voltage" should differ from the initial gate voltage by an amount equal to the initial gate voltage of -10 V. The average increase actually obtained was -8.5 V with a standard deviation of 1.42 V. These results indicate that the oxide charging reaches approximately 85 percent of its final value in 1 minute under the conditions stated.

It would be of value to obtain an easy method of determining both  $N_t$  and the constant "A" in Figure 6. The change in threshold voltage in terms of saturation of all available traps can be written as:

$$\Delta V_t \text{ (sat)} = \frac{q X}{\epsilon_{ox} \epsilon_o S} A \quad (\text{Eq. 4})$$

where X is the distance from the centroid of the charge to the gate metal (approximated by  $d_{ox}$ ), A is the initial trapping probability and S is the capture cross section. For avalanche hole injection:

$$\Delta V_t \text{ (sat)} = \Delta V_G \quad (\text{Eq. 5})$$

Taking the typical value of S as  $5 \times 10^{-14} \text{ cm}^2$ , the "A" value for the oxide can be calculated as:

$$A = \frac{\Delta V_G \epsilon_{ox} \epsilon_o (5 \times 10^{-14} \text{ cm}^2)}{q X} \quad (\text{Eq. 6})$$

where X may be approximated by  $d_{ox}$  in some cases.

A typical  $\Delta V_G$  obtained with the test devices was 20 V. Assuming  $d_{ox} = 0.1 \text{ } \mu\text{m}$ :

$$A = \frac{(30 \text{ V}) (3.9) (8.854 \times 10^{-12} \text{ Fm}^{-1}) (5 \times 10^{-18} \text{ M}^2)}{(1.602 \times 10^{-19} \text{ coulomb}) (0.1 \times 10^{-6})} \quad (\text{Eq. 7})$$

$$A = 0.215$$

which is the A value for a moderately soft oxide. The total number of oxide traps is estimated as:

$$N_t = \frac{(20 \text{ V}) (3.9) (8.854 \times 10^{-12} \text{ Fm}^{-1})}{(1.602 \times 10^{-19} \text{ coulomb}) (0.1 \times 10^{-6} \text{ m})} \quad (\text{Eq. 8})$$

$$N_t = 4.31 \times 10^{12} \text{ traps/cm}^2$$

which is consistent with the known properties of oxides.

## 8. IMPROVEMENTS

A decisive verification of avalanche hole injection will require tests on known hard and soft oxides. The variation in hardness of a sample of commercial parts may be too small for the avalanche hole technique to resolve.

The test parts should be irradiated at low doses to avoid the effects of surface states. When used as a screen, surface state effects will have to be factored in separately.

It is possible to improve the avalanche hole injection technique. If the small oxide current could be successfully measured, it would be possible to estimate the capture cross section of the hole traps.

Maier\* has suggested that the surface states produced by avalanche hole injection may be measured by noting the increase in the junction leakage current produced by the stress. A gated diode can be used to make this measurement by depleting the surface under the gate and noting

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\*Private Communication with Roe Maier of AFWL.

the increase in leakage current. No such increase was observed when attempting to use the 40468A as a gated diode. The observed leakage current (nanoamps) is probably due to package leakage and bulk recombination currents which are much larger in magnitude than the surface generation current component.

It is suggested that in phase II, the p-n junction avalanche technique be applied to a gated diode, for which both the  $\Delta V_G$  to maintain a constant breakdown voltage and the increase in surface recombination velocity,  $\Delta I_{SO}$ , can be monitored as a function of stress.

In conclusion, the avalanche hole injection technique has not been verified as a functional screen for parts to be subjected to a total dose environment. However, reasons have been given why these results should not be considered conclusive. Values of the total number of traps and the initial trapping probability were calculated for a typical test device which are consistent with the known properties of gate oxides. The computed oxide parameters predict that the RCA 40468A possesses a moderately soft oxide.

The avalanche hole injection technique may still prove to be a valid simulation of the radiation environment if applied to a gated diode structure and evaluated over a range of stress conditions and radiation levels.

### SECTION III

#### NEGATIVE BIAS TEMPERATURE STRESS (NBT)

##### 1. OBJECTIVE

The purpose of the NBT experiment is to determine the degree of correlation between damage produced by NBT and damage produced by total ionizing dose.

##### 2. RATIONALE

Several studies (refs. 5, 6) have investigated the effects of heating MOS devices with a negative bias applied to the gate. The investigators found that NBT treatment increased the surface state density and the density of positive charge. Jeppson and Svensson (ref. 7) suggest that at low electric fields, stress activates a chemical reaction which produces a positive oxide charge and a surface defect, while at high electric fields, holes are injected from the semiconductor and the trapped holes create surface states.

Because NBT and total dose both produce similar damage, i.e., trapped holes and interface states, NBT stress may act as a substitute for radiation tests. Such a substitution, if possible, could save significant amounts of time and expense by eliminating the need for radiation testing, except perhaps on a periodic basis.

##### 3. JUSTIFICATION

NBT is not the only possible "radiation simulator" technique possible. Hole injection by p-n junction avalanche (discussed previously) is a room temperature technique but produces such a narrow region of damage that device electrical characteristics are virtually unaffected. Bulk avalanche-

ing techniques can also be done at room temperature but only with complex equipment on a specially fabricated test structure. NBT, while requiring high temperatures, is simple and can be performed on any gated device which has no input protection network.

#### 4. PROCEDURE

The experimental procedure chosen was to subject N-channel MOSFETs to a low-field NBT treatment. The first group of samples were stressed at  $300\frac{1}{2}^{\circ}\text{C}$  for 15 minutes with a gate bias of -20 volts and all other leads grounded. The damage was then annealed out at  $300\frac{1}{2}^{\circ}\text{C}$  for 1 hour with all leads shorted. The devices were then irradiated under bias  $1 \times 10^6$  Rad (Si) by exposure to  $\text{Co}^{60}$ . The correlation between the change in threshold voltage induced by NBT and the change in threshold voltage produced by the irradiation was determined.

#### 5. SAMPLES

RCA 40468A MOSFETs were used as test vehicles in the experiment. The 40468A is an N-channel depletion mode DMOS device which has no gate protection network.

#### 6. ELECTRICAL TESTS

Threshold voltage for the samples was determined by plotting the drain current versus gate voltage with a drain voltage of 50 mV. Threshold voltage was obtained by extrapolating along the line segment where transconductance is a maximum to the  $I_D = 0$  line. The slope of the straight line segment is directly proportional to the maximum field effect mobility.

## 7. IRRADIATION

Devices were irradiated on the AFWL 5 kilocurie  $\text{Co}^{60}$  gamma ray source. A gate bias of +1V was applied during the irradiation and all other leads were grounded.

## 8. DATA ANALYSIS

Figure 7 is a plot of the change in threshold voltage due to radiation ( $\Delta V_{TR}$ ) as a function of the change in threshold voltage caused by NBT ( $\Delta V_{TS}$ ). A least squares fit is drawn through the data. The correlation coefficient is  $0.83 \pm 0.14$ . Relevant statistics for this test are given in Table 2.

Table 2  
TEST RESULTS

|           | <u>Prestress <math> V_T </math></u> | <u><math> \Delta V_T </math> NBT</u> | <u><math>V_T(\text{Prestress})/V_T(\text{Anneal})</math></u> | <u><math> \Delta V_T  \text{ RAD}</math></u> |
|-----------|-------------------------------------|--------------------------------------|--|--|
| $\bar{X}$ | 1.46 V                              | 0.18 V                               | 0.97   | 2.11 V                                       |
| $\sigma$  | 0.086                               | 0.19                                 | 0.078  | 0.61   |
| n         | 10                                  | 7                                    | 7  | 7  |

Encouraged by these results, the experiment was repeated for an additional 15 test devices with some variations intended to improve the correlation. The NBT stress time was doubled to 30 minutes to attempt to produce a more substantial level of damage. More points were measured on the drain current versus gate voltage characteristic curves so  $|V_T|$  could be measured with greater accuracy. The anneal bake was lengthened to 6 hours in an attempt to make the ratio  $[\text{Prestress } |V_T| / \text{Anneal } |V_T|]$  more closely approach unity. The radiation level was reduced to  $1 \times 10^5$  Rad (Si) so that the change in threshold voltage produced by irradiation would be comparable to the change caused by NBT. The statistical results of this experiment are given in Table 3 ( $m$  = transconductance).

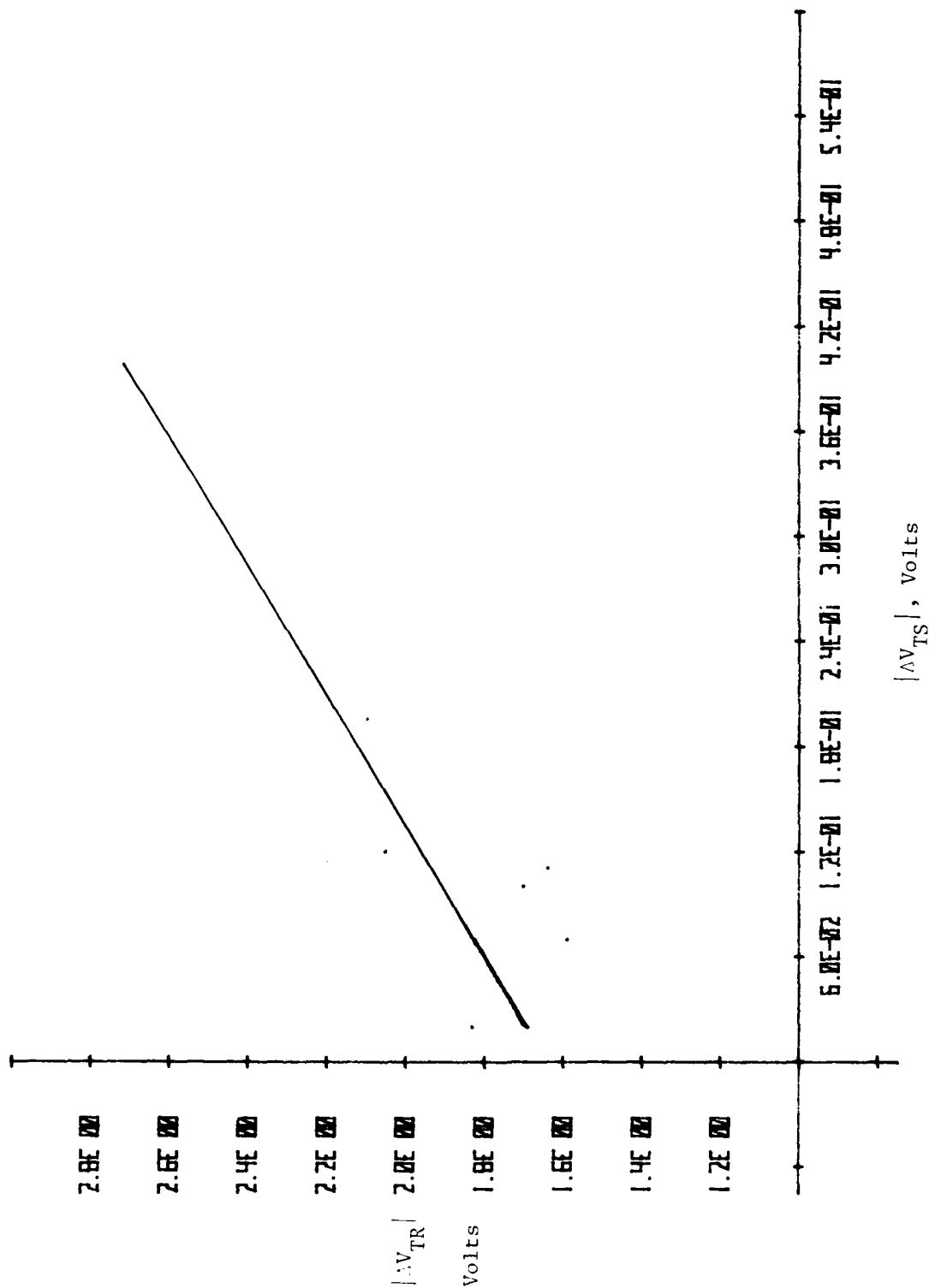


Figure 7. Radiation Induced Change in Threshold Voltage as a Function of the Stressed Induced Change in Threshold Voltage.  $R = 0.83 \pm 0.14$

TABLE 3. TEST RESULTS

|           | <u>Initial</u> |                        | <u>NBT</u>     |                       | <u>Anneal</u>                              |  | <u>Radiation</u> |                        |
|-----------|----------------|------------------------|----------------|-----------------------|--|--|------------------|------------------------|
|           | $ V_T $        | $ m $                  | $ \Delta V_T $ | $ \Delta m $          | $ V_T(\text{Initial})/V_T(\text{Anneal}) $ | $ m(\text{Initial})/m(\text{Anneal}) $ | $ \Delta V_T $   | $ \Delta m $           |
| n         | 15             |                        |                | 15                    |  | 15                                     |                  | 15                     |
| $\bar{X}$ | 1.47 V         | 250.13 $\mu\text{mho}$ | 0.137 V        | 67.33 $\mu\text{mho}$ | 0.984                                      | 1.04                                   | 1.27 V           | 142.33 $\mu\text{mho}$ |
| Max       | 1.77           | 315                    | 0.27           | 175                   | 1.007                                      | 1.17                                   | 1.52             | 167                    |
| Min       | 1.38           | 167                    | 0.06           | -15                   | 0.953                                      | 0.75                                   | 1.04             | 34                     |
| $\sigma$  | 0.10           | 45.68                  | 0.049          | 48.91                 | 0.015                                      | 0.10                                   | 0.130            | 31.6                   |

The ratio of  $|V_T|$  initial to  $|V_T|$  anneal for the 1 hour anneal was 0.97 with a standard deviation of 0.078. The annealing ratio for the 6-hour anneal was 0.984 with a standard deviation of 0.015, indicating that a 6-hour 300°C bake produced better anneals than the 1-hour bake.

A plot of  $|V_T(\text{initial}) - V_T(\text{NBT})|$  as a function of  $|V_T(\text{anneal}) - V_T(\text{Rad})|$  is shown in Figure 8. The correlation coefficient between the two parameters was found to be  $-0.30 \pm 0.25$ .

Because of the relatively large degradation in the field effect mobility produced by both NBT and radiation, this parameter was also studied. Figure 9 is a plot of the change in maximum transconductance produced by NBT as a function of the change in maximum transconductance produced by radiation. The correlation coefficient is  $-0.12 \pm 0.27$ .

## 9. DISCUSSION

The correlations obtained for the more tightly controlled experiment are discouraging. However, explanations for these results suggest NBT may yet prove useful.

The large changes in transconductance suggest that surface state creation is dominating the radiation response. Surface state domination can produce threshold voltage shift turnabout, as illustrated by Figure 10. If NBT produces damage equivalent to dose  $X_1$  of Figure 10 and the irradiation level is at dose level  $X_2$ , the nonlinear characteristic will reduce the correlation between NBT and radiation.

Other factors may also be responsible for the poor correlations obtained. NBT causes a hole flux to flow from the semiconductor toward the metal while the positive voltage applied during irradiation produced a hole flux in the opposite direction. Except for the case of hole trap saturation, the two fluxes should produce slightly different charge centroids. Negative gate biases also have a characteristic saturated threshold voltage different than that of positive gate biases. This saturated threshold voltage occurs when compensating charges built up

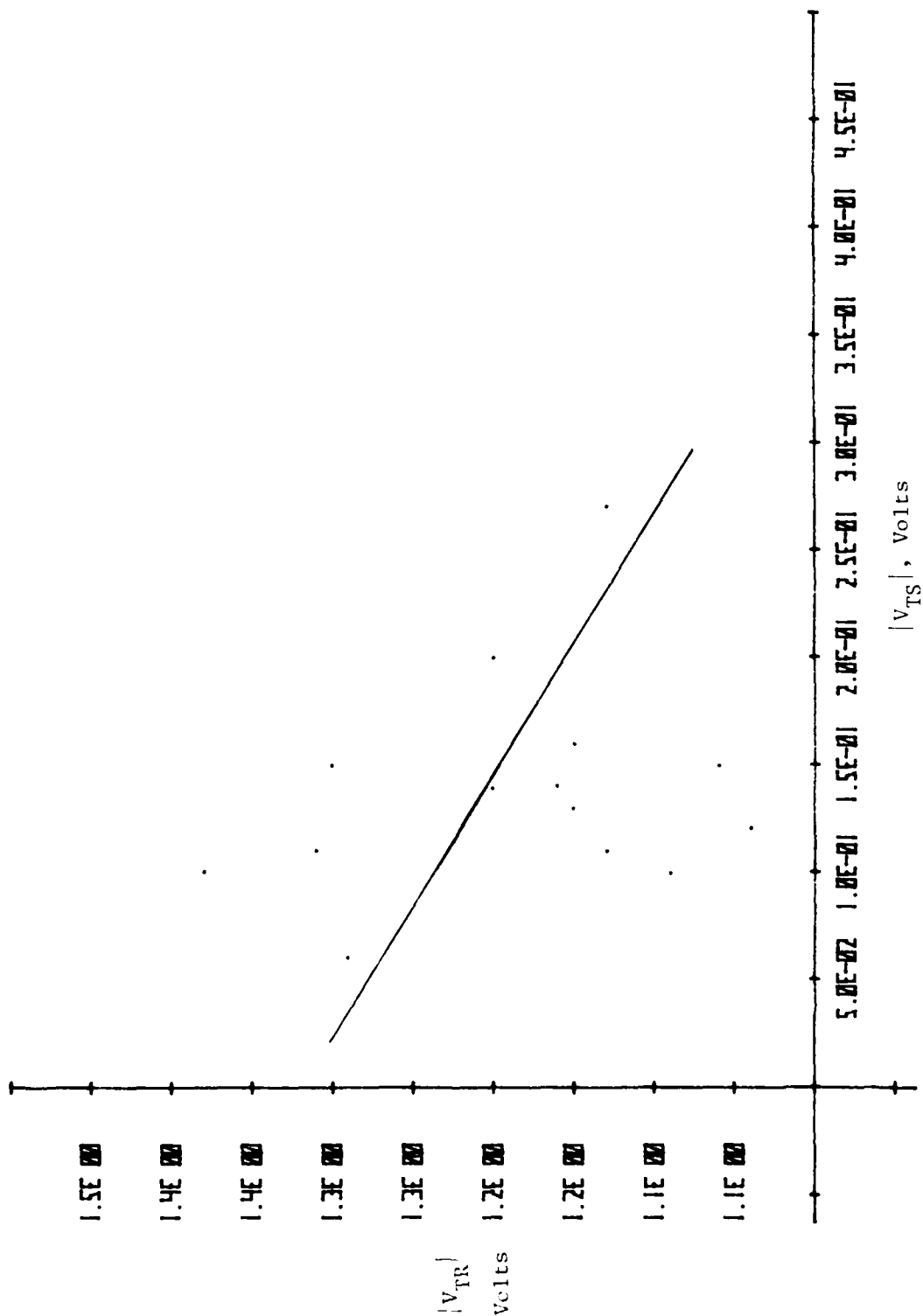


Figure 8. Change in Threshold Voltage Produced by Stress as a Function of Stress Induced Threshold Voltage Change  $R = -0.304$

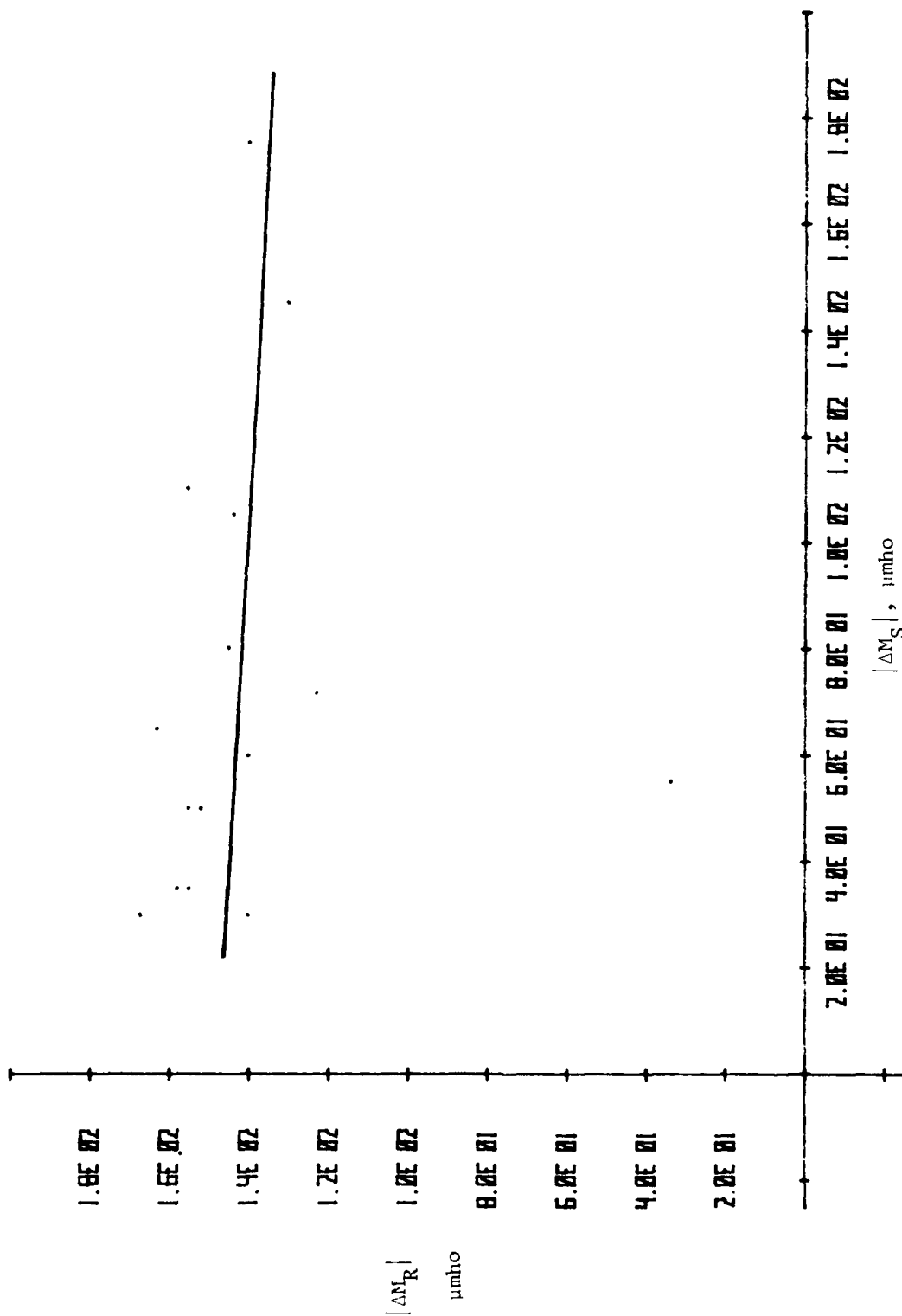


Figure 9. Radiation Induced Change in Transconductance as a Function of the Stress Induced Changed in Transconductance.  $R = -0.121 \pm 0.27$

in the oxide cause the electric field to vanish. In addition, the high temperatures utilized for NBT may alter the physical constants and dynamics of the trapping process. Finally, it has not been established whether the high field or low field regime is the more suitable of radiation. NBT effects will occur over a wide range of temperatures and electric fields.

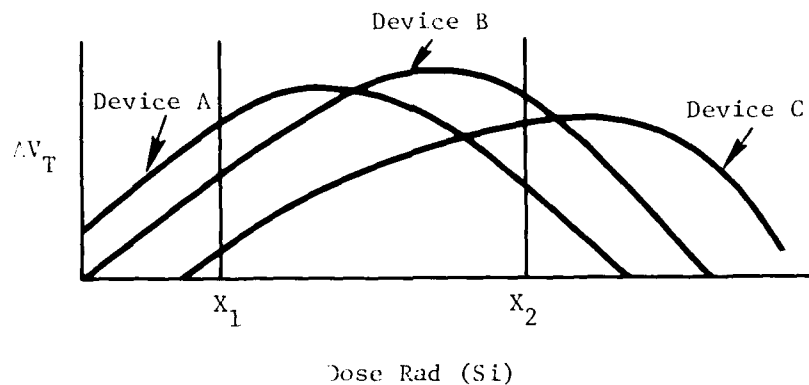


Figure 10. Turnabout Produced by Surface States

#### 10. IMPROVEMENTS

In the phase II verification tests for NBT,  $\Delta V_T$  versus stress time will be performed at both high and low electric field strengths. These will be compared to the "growth" curves for  $\Delta V_T$  vs  $\gamma$ . In addition, p-channel devices will be investigated. Tests will also be performed on p and n substrate MOS capacitors to determine if the capacitor structure may prove a better test vehicle for this technique.

#### SECTION IV

#### $H_{FE}$ DEGRADATION FROM EMITTER - BASE (E-B) STRESS

##### 1. OBJECTIVE

The purpose of this experiment is to determine if gain degradation produced by E-B stress is correlated to gain degradation produced by total ionizing dose.

##### 2. RATIONALE

Several studies (refs. 8, 9, 10) have shown that avalanche breakdown of the base-emitter junction in bipolar transistors produces energetic holes which may be injected into the base oxide, producing surface damage similar to the damage produced by ionizing radiation. Hole injection produces an increase in the density of surface states in the base, which act as recombination centers, and positive oxide charges, which alter the surface potential. Current gain degradation is the major effect produced in transistors after accumulation of a total ionizing dose.

Transistor susceptibility to gain degradation produced by total ionizing dose should be related to the gain degradation produced by E-B stress, if the hole injection process can be controlled by a gate electrode over the base oxide. In the absence of a gated base, injection may still occur but will be controlled by the naturally occurring surface fields, whose magnitudes are not known.

##### 3. JUSTIFICATION

Because gated devices were not available for the verification phase, E-B stress was applied to commercial bipolar transistors to determine if the natural surface fields would produce a controlled injection and allow E-B stress to be used as a sample part screen for commercial packaged devices.

#### 4. PROCEDURE

For the experimental test procedure, a sample of packaged transistors was chosen as test structures. These transistors were then subjected to the following procedures:

- (1) Pretest Electrical Characterization
- (2) Stabilization Bake at 280°C for 10 minutes
- (3) Poststabilization Electrical Characterization
- (4) Emitter-Base Stress
- (5) Poststress Electrical Characterization
- (6) Anneal Bake for 6 Hours at 275°C
- (7) Postanneal Electrical Characterization
- (8) Gamma Irradiation to  $0.5 \times 10^6$  Rad (Si)
- (9) Postradiation Electrical Characterization

The purpose of the device stabilization was to ensure that changes which occurred during the high temperature bake were due only to the damage annealed out during the stress step. The poststabilization and postanneal characteristics serve as baselines which are nearly equal for measuring damage produced by stress and radiation.

#### 5. SAMPLES

Forty transistors of 4 device types were tested in this verification test. The transistors included 10-2N2720 NPN low power, 10-2N2944 PNP low power, 10-2N3468 PNP high power and 10-2N2537 NPN switching transistors. All transistors were encapsulated in metal packages.

#### 6. ELECTRICAL TESTS

Recombination centers introduced into the base region will not alter the injection of minority carriers into the base region and thus will have no effect on collector current. However, the recombination of minority

carriers in the base will result in an increase in base current. This additional base current component is especially important at low collector currents where surface recombination can become the dominant factor determining current gain. Therefore, base current at a constant value of collector current was determined at each electrical characterization step. The values of collector current at which base current was measured were 10  $\mu$ A, 100  $\mu$ A, 1 mA, and 10 mA. Measurements were made on a Tektronix 577 curve tracer with a collector to emitter voltage of 6.5 volts.

All devices except the 2N2944 were stressed for 1 minute by avalanching the base-emitter junction at 10 mA and leaving the collector open. The 2N2944 was stressed at 1 mA for 1 minute to keep the power dissipation caused by the high base-emitter breakdown voltage at acceptable levels.

## 7. IRRADIATION

The test devices were irradiated by exposure to the AFWL 5 kilocurie  $\text{Co}^{60}$  gamma ray source. The test devices were irradiated to a total ionizing dose of  $5 \times 10^5$  Rad (Si). All devices were irradiated with a collector-base reverse bias of 10 volts. The base and emitter leads were grounded.

## 8. RESULTS

A summary of device behavior throughout the test sequence will be given in terms of the base current required to maintain a collector current of 100  $\mu$ A.

The stabilization bake caused the base current of some devices to increase while other devices showed a decrease. A summary of device behavior following the bake is shown in Table 4.  $\bar{I}_B$  is the post-bake average base current.  $F_{INC}$  is defined as:

$$\frac{I_B \text{ (Stabilization)}}{I_B \text{ (Initial)}} \quad (\text{Eq. 9})$$

for the device which produces the largest quotient.  $F_{DEC}$  also uses equation 9, but this number is for the device with the smallest quotient.

Table 4  
EFFECT OF STABILIZATION

| Device | $\bar{I}_B$  | $F_{INC}$ | $F_{DEC}$ |
|--------|--------------|-----------|-----------|
| 2N2720 | 268 nA       | 1.03      | 0.92      |
| 2N2944 | 351 nA       | 1.06      | 0.99      |
| 2N3468 | 2.59 $\mu$ A | 1.01      | 0.93      |
| 2N2537 | 5.89 $\mu$ A | 1.85      | 0.77      |

Similar results for the base current following stress are shown in Table 5.  $F_{INC}^S$  is defined as:

$$\frac{I_B \text{ (Stress)}}{I_B \text{ (Stabilization)}} \quad (\text{Eq. 10})$$

for the device which produces the largest value.  $F_{DEC}^S$  describes the device with the smallest change.

Table 5  
EFFECT OF STRESS

| Device    | $I_B$        | $F_{INC}^S$ | $F_{DEC}^S$          |
|-----------|--------------|-------------|----------------------|
| 2N2720NPN | 552 nA       | 2.96        | No decrease observed |
| 2N2944PNP | 481 nA       | 2.30        | No decrease observed |
| 2N3468PNP | 2.69 $\mu$ A | 1.09        | 0.995                |
| 2N2537NPN | 3.20 $\mu$ A | 1.91        | 0.49                 |

The surprising result of Table 5 is that stress can produce an increase in current gain. This anomalous gain increase has been attributed to injected positive charge bringing the silicon surface in the base region out of depletion, where maximum recombination occurs.

The purpose of the annealing step was to bring the electrical characteristic back to the poststabilization values. Table 6 is a summary of the annealing results.  $\Delta \bar{I}_B$  of Table 6 is equal to the post anneal average base current minus the poststabilization average base current.  $F_{INC}^A$  and  $F_{DEC}^A$  are the largest and smallest values of:

$$\frac{I_B (\text{Anneal})}{I_B (\text{Stabilization})} \quad (\text{Eq. 11})$$

Table 6  
ANNEAL RESULTS

| Device | $\bar{I}_B$  | $\Delta \bar{I}_B$ | $F_{INC}^A$ | $F_{DEC}^A$ |
|--------|--------------|--------------------|-------------|-------------|
| 2N2720 | 305 nA       | 38 nA              | 1.30        | None*       |
| 2N2944 | 385 nA       | 34 nA              | 1.16        | None        |
| 2N3468 | 2.78 $\mu$ A | 0.19 $\mu$ A       | 1.14        | None        |
| 2N2537 | 6.12 $\mu$ A | 0.23 $\mu$ A       | 1.19        | 0.93        |

\*None - No device had an  $\frac{I_B (\text{Anneal})}{I_B (\text{Stabilization})} < 1$

Table 6 indicates that, in almost all cases, the stress damaged transistors cannot recover to their prestress current gain values by applications of an anneal cycle. However, annealing did reduce damage significantly.

To be effective as a screen, the level of damage produced by stress should correlate with the damage caused by the radiation exposure. Figures 11a-d are plots of the change in one over gain between the stabilized parts and the stressed parts, as a function of the change in one over gain between the annealed parts and the irradiated parts for each device type.

Figure 11a, the plot of  $\Delta I/\beta_s$  as a function of  $\Delta I/\beta_y$  for the 2N3468, produces a least squares fit to the data with a correlation coefficient of  $-0.11 \pm 0.35$ , or no correlation at all. Figure 11b shows a correlation coefficient between stress and radiation damage of  $0.64 \pm 0.21$ . Gross features of Figure 11b, however, are discouraging. One device which showed the next to the lowest change of stress induced damage showed the highest level of radiation induced damage. Figure 11c produced a correlation coefficient of  $-0.64 \pm 0.21$  which opposes the model these tests are designed to support. Figure 11d gives no indication that the devices with the highest stress induced damage show high levels of radiation induced damage.

## 9. CONCLUSIONS

It is obvious that the emitter-base stress test as conducted is unsuitable as a screen. However, this result is not totally unexpected because of the inability to control the hole injection without a gated base region. With a base electrode, greater control of the hole injection would be possible. In addition, a base current versus gate voltage curve could be generated which would allow the effects of positive charges in the base oxide to be predicted.

STRESS VERSUS RADIATION  
INDUCED DAMAGE FOR  
THE 2N3468

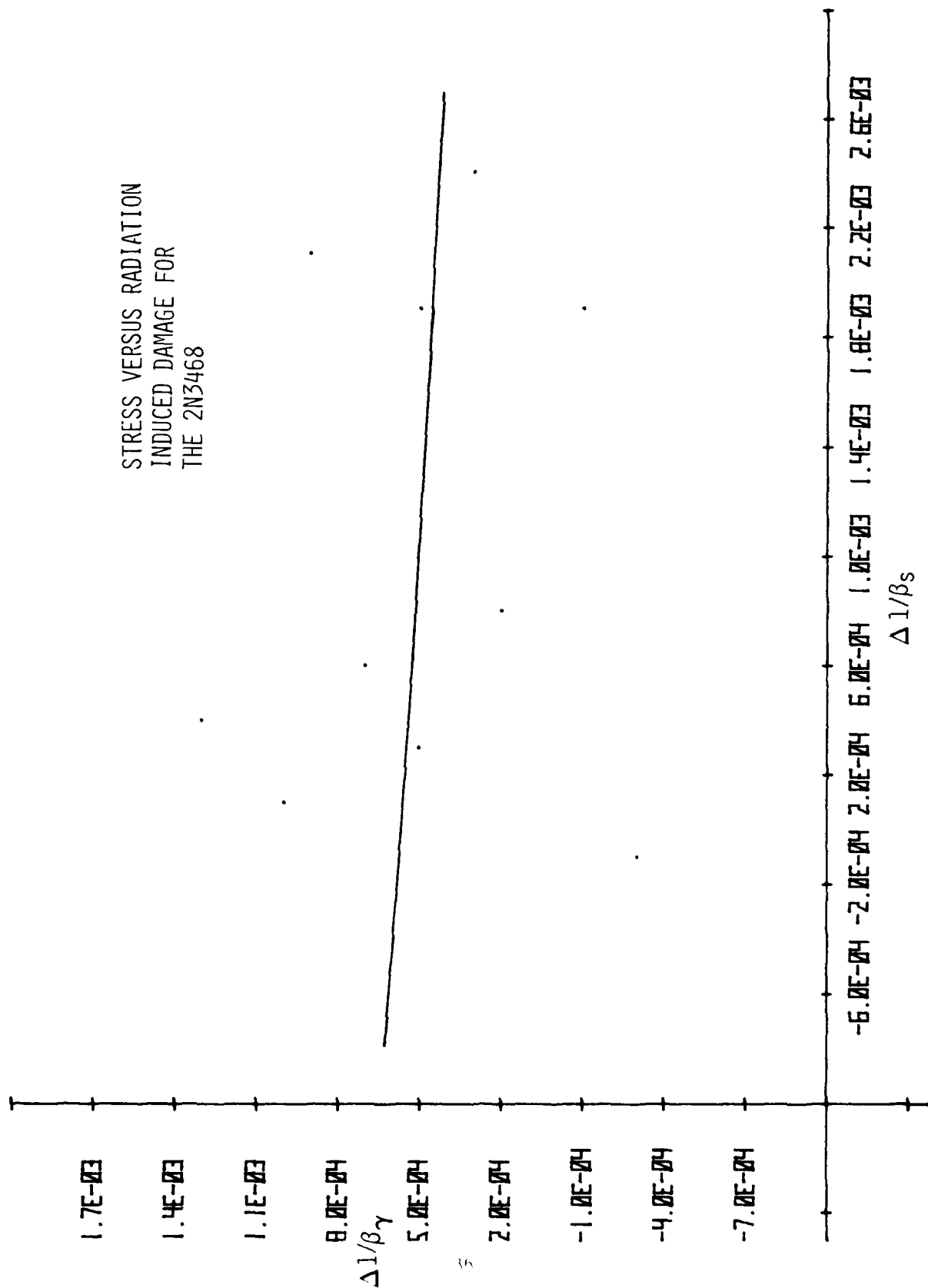


Figure 11a. Stress Versus Radiation Induced Damage for 2N3468.  $R = 0.11 \pm 0.35$

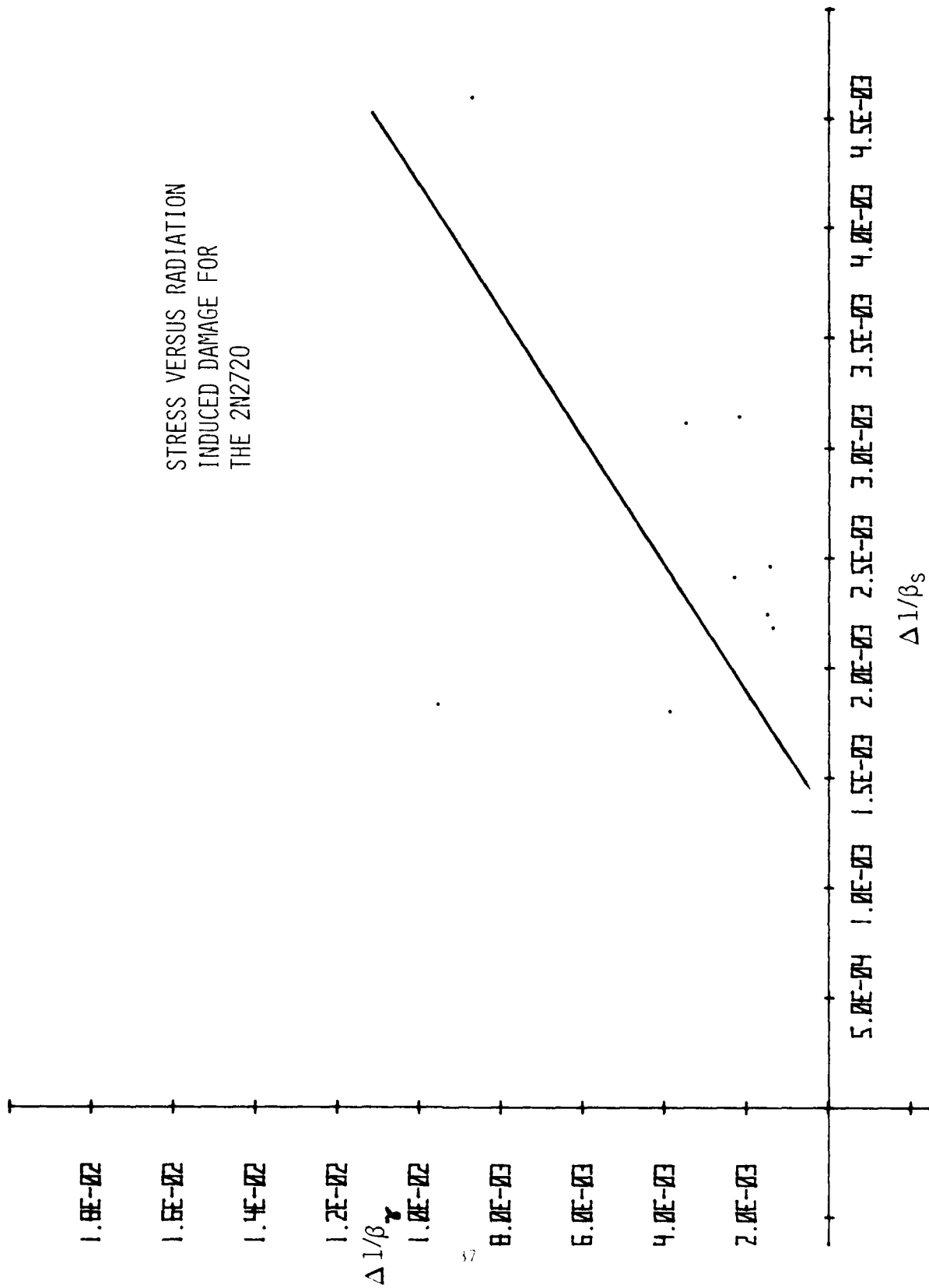


Figure 11b. Stress Versus Radiation Induced Damage for the 2N2720.  $R = 0.64 \pm 0.21$

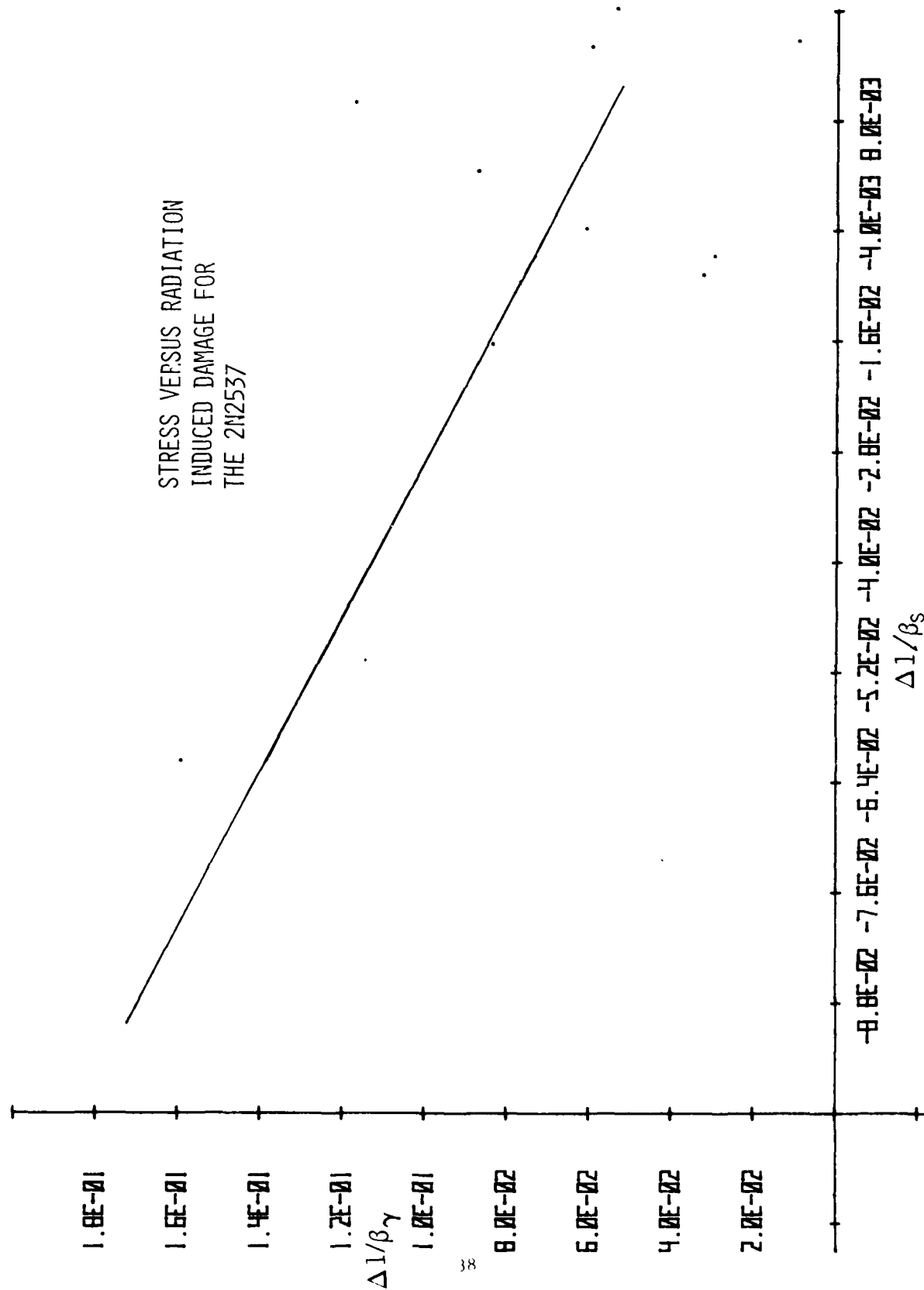


Figure 11c. Stress Versus Radiation Induced Damage for the 2N2537.  $R = -0.64 \pm 0.21$

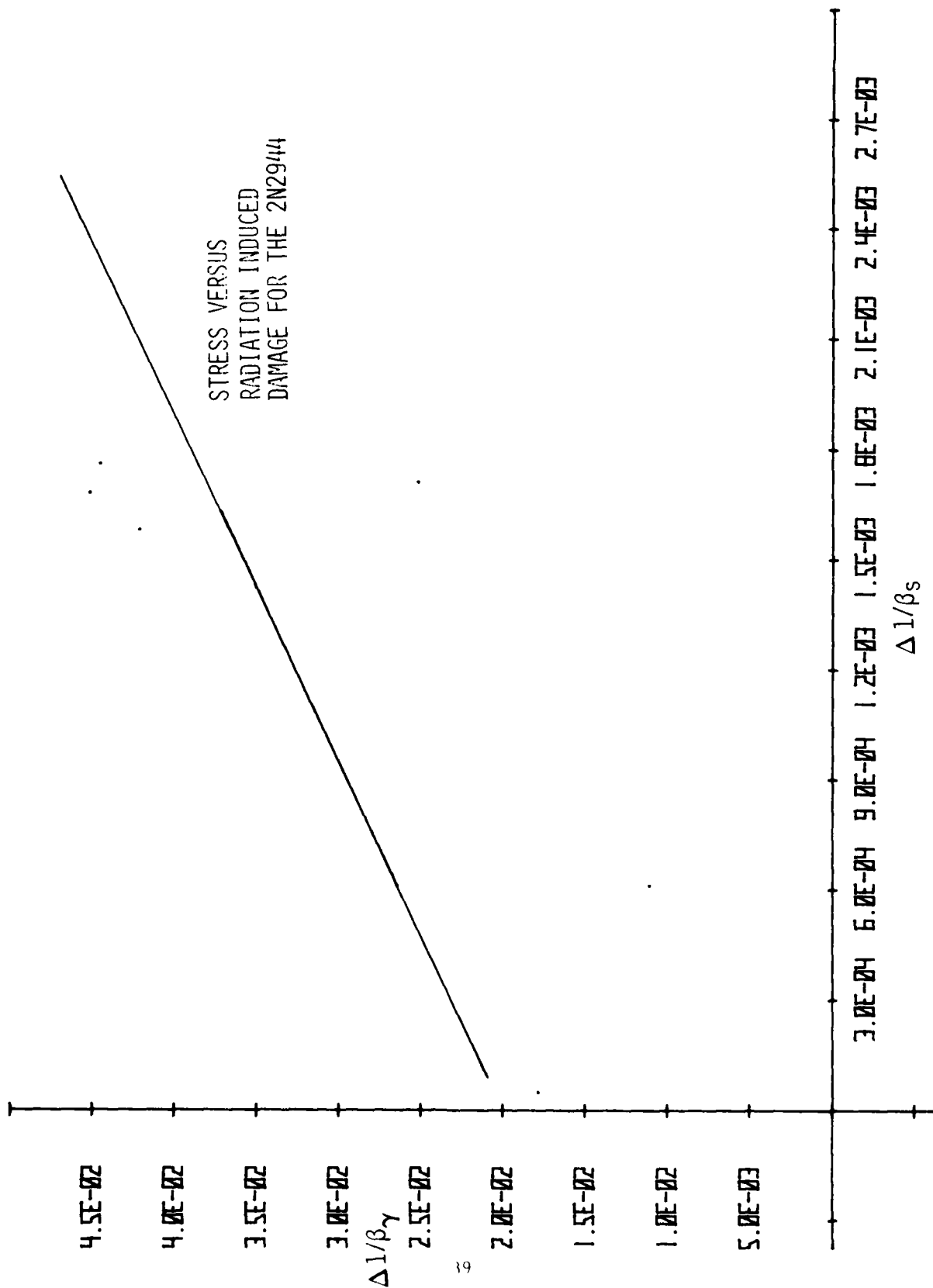


Figure 11d. Stress Versus Radiation Induced Damage for the 2N2944.  $R = 0.62 \pm 0.22$

## SECTION V

### EDGE STATES BY NOISE MEASUREMENTS

#### 1. OBJECTIVE

The purpose of this experiment was to determine if a correlation exists between the density of edge states near the band edge and the radiation susceptibility of a device to total ionizing dose. Surface states density was inferred from measurements of electrical noise.

#### 2. RATIONALE

Evidence has been presented by Pepper (refs. 11, 12) that the oxide hole trap consists of a dipole charge near the oxide-semiconductor interface in the oxide layer. Because of the weak field of dipoles, they would be expected to produce interface states with very shallow levels.

Sah and Hielscher (ref. 13) found that the square of the low frequency electrical noise at the gate of an MOS structure is directly proportional to the density of surface states with energies at the Fermi level. By adjusting the Fermi level close to the band edge, the shallow energy states produced by dipoles may become the dominant noise voltage term. The square of the noise voltage would then be related to the number of oxide hole traps.

#### 3. JUSTIFICATION

Other methods of surface state measurement were considered but rejected. The C-V method was rejected because it must be performed at the wafer probe level and it is only accurate in the midgap region. The method utilized by Pepper of measuring the effect of substrate bias on

conductivity was considered impractical because temperatures of 4.2°K were required. Hall effect measurements required special test structures and equipment.

The advantage of noise measurements is that they can be made using commercial equipment. Also, measurements can be made in inversion on packaged MOSFETs.

#### 4. PROCEDURE

The procedure used to measure edge states was to measure the equivalent gate noise of MOS transistors in strong inversion. In strong inversion, the Fermi level can be expected to be within a few tenths of an eV of the band edge. Any voltage drop across the channel should be minimized so the Fermi level will be uniformly constant within the device. The noise measurement must be made at a low frequency ( $< 20$  Hz) to insure detection of states with slower time constants. Following irradiation of the test devices, the square of the low frequency noise can be compared to the change in threshold voltage produced by the radiation.

#### 5. SAMPLES

The test samples used in this experiment were RCA 40468A MOS transistors. These devices are N-channel depletion mode DMOS with no gate protection.

#### 6. ELECTRICAL TESTS

Low frequency gate noise of the test samples was measured using a HP4470A Transistor Noise Analyzer. The 4470A was utilized because it is one of the few commercial instruments suitable for measuring MOSFET noise. Systems such as the one used by Sah (ref. 13), which can make measurements across the band gap, were not fabricated due to program constraints.

The drain voltage was maintained at the smallest possible value (68 mV) that the HP4470A would allow. Drain current was set to 100  $\mu$ A. The equivalent RMS gate voltage at 10 Hz at a bandwidth of 1 Hz was read directly from a panel meter.

The threshold voltage of the test devices were measured in the linear region by plotting drain current as a function of gate voltage with a drain voltage of 50 mV.  $|V_T|$  was obtained by extrapolating along the line segment where transconductance is a maximum to the  $I_D = 0$  line.

#### 7. IRRADIATION

The devices were irradiated by exposure to the AFWL 5 kilocurie  $\text{Co}^{60}$  source. The total dose received was  $1 \times 10^6$  Rad (Si). The gates were biased at +1V during the irradiation and all other leads were grounded.

#### 8. RESULTS

The squared noise voltage plotted as a function of change in threshold voltage is shown in Figure 12.

The correlation coefficient of  $0.22 \pm 0.34$  and features of the plot indicate that low frequency gate noise will not predict threshold voltage shift of MOSFETs at a dose level of  $1 \times 10^6$  Rad (Si).

#### 9. ANALYSIS

There are several reasons for the poor results. If the  $(\text{noise})^2$  measured was proportional to the dipole density, a poor correlation could result due to the nonlinear damage characteristic observed at the higher doses. To be conclusively tested for value as a screen, the test samples would have to include hard and soft oxides, with irradiation levels kept low.

The most likely explanation for the poor correlation is that the electrical noise observed was not from dipole charges but from other

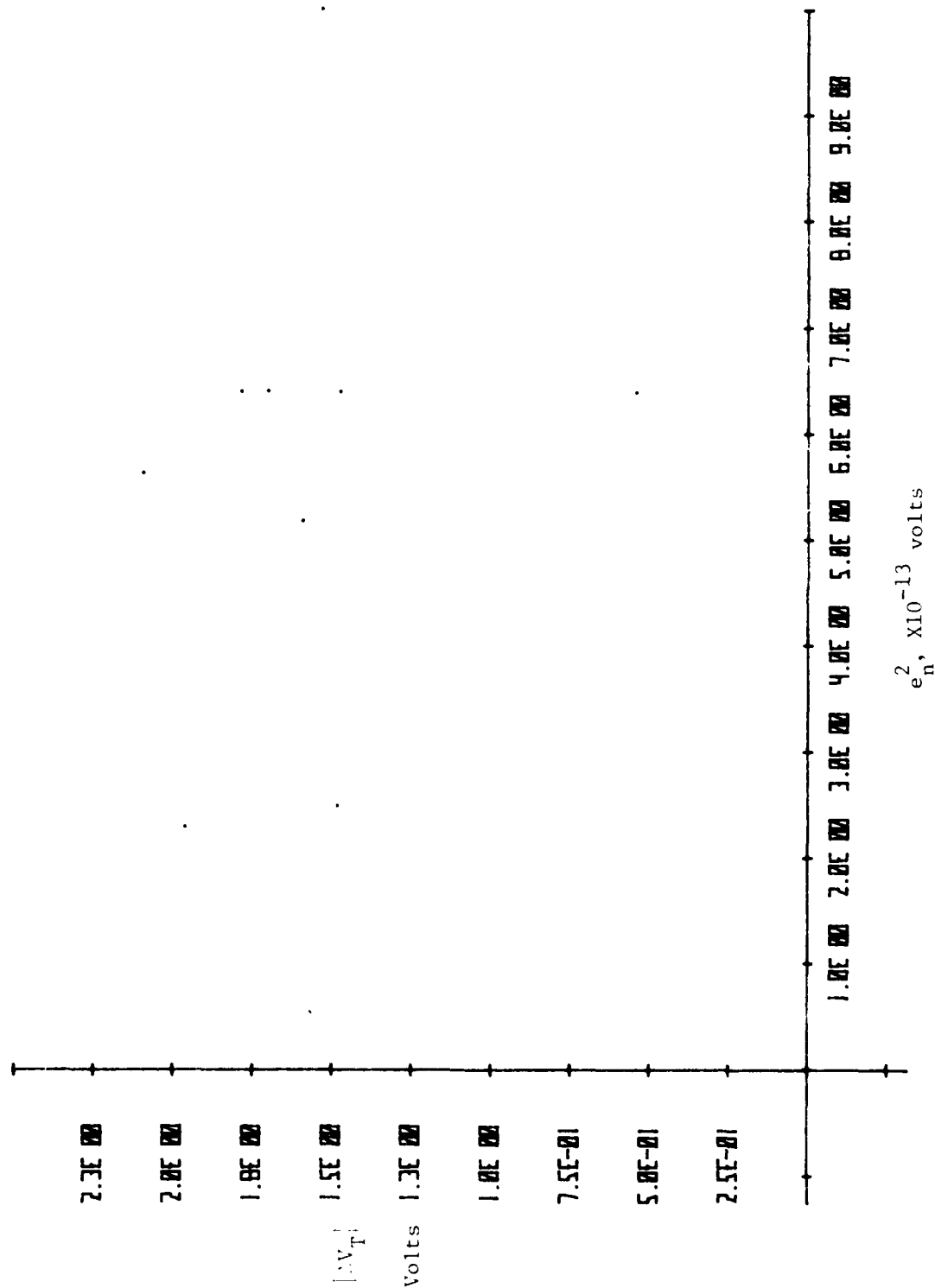


Figure 12. Threshold Voltage Shift as a Function of Equivalent Gate Voltage.  $R = -0.22 \pm 0.34$

sources. The necessity of biasing the transistors on produces an additional noise source as indicated by Aoki, Katto, and Yamada (ref. 14). Aoki et al., have found that conductance mobility fluctuations due to surface potential roughness contribute to noise. However, Aoki concludes that "measurements of  $1/f$  noise at low current levels will provide an effective means of monitoring various processes." Pepper (ref. 15) concludes that "the potential fluctuations due to the pairs are weak and consequently they do not show up in conventional C-V or G-V techniques." Pepper's remarks suggest that it may be impossible to detect hole trap dipoles using a room temperature measurement.

Because of the rapid falloff of the electric field produced by dipoles, only those dipoles very near the interface can be expected to produce surface states. Hole traps deep in the oxide may go undetected.

## 10. CONCLUSIONS

For edge state determinations to be useful as a screen, it first must be established that the shallow surface states produced by hole trap dipoles can be detected at room temperature. If these states can be detected, then noise measurements will be useful if (1) the noise in strong inversion is dominated by these charges and (2) the dipole density at the interface is an indicator of the oxide hardness.

To conclusively verify the value of noise measurements, hard and soft oxides should be evaluated and all radiation tests conducted at low levels.

## SECTION VI

### DETECTION OF DIPOLE CHARGE

#### 1. OBJECTIVE

The objective of this experiment was to correlate the relative magnitude of total oxide charge measured by noise techniques to the radiation susceptibility of test devices. It was hypothesized that the total oxide charge may include dipole charge associated with hole traps.

#### 2. RATIONALE

Pepper (ref. 15) has given evidence that the hole trap consists of a dipole charge in the oxide. Nicollian and Melchior (ref. 16) have shown that oxide charges alter the surface potential in local regions. The distribution of surface potential affects the spectrum of noise in a manner which allows calculation of  $\sigma$ , the standard deviation of surface potential.  $\sigma$ , in turn is related to  $Q$ , the total oxide charge. If the oxide total charge includes Pepper's dipoles, then determination of  $\sigma$  should act as a hardness assurance screen.

#### 3. PROCEDURE

To obtain  $\sigma$ , the log of the squared noise voltage is plotted against the log of frequency. An asymptote of slope 0 is fit to the low frequency data, which should approach a zero slope. Another asymptote of slope  $1/f$  is fit to the higher frequency data and is tangent to the data at the point  $F_p$ . The intersection of the two asymptotes occurs at the point  $F_L$ . Taking the frequency values of  $F_p$  and  $F_L$ ,  $\sigma$  can be approximated from:

$$F_L = F_p \exp [-(\pi^2)^{1/2} \sigma] \quad (\text{Eq. 12})$$

#### 4. SAMPLES

Ten RCA 40468A MOSFETs were evaluated using noise measurements. The 40468A is an N-channel depletion mode DMOS device with no gate protection.

#### 5. ELECTRICAL TESTS

The HP4470A Transistor Noise Analyzer was used to obtain the noise spectrum data. Drain voltage and drain current were picked to maximize the bandwidth over which measurements could be made.

#### 6. RESULTS

Unfortunately, the bandwidth of the HP4470A Transistor Noise Analyzer was not sufficient to accurately determine  $F_L$  and  $F_p$  as indicated by Figure 13. No line segment with slope of either 0 or  $1/f$  can be resolved within the band of frequencies accessible. Therefore, determination of  $\sigma$  from the HP4470A measurements does not appear feasible.

#### 7. IMPROVEMENTS

R. Maier\* has suggested that  $\sigma$  can also be obtained from the spread of the conductance versus frequency curve for MOS capacitors. Preliminary work is being done in this area, but no results are available for presentation.

Another possible area of investigation is based on the work of Aoki, Kato and Yamada (ref. 14). Aoki et al. noted that the noise of "on" MOSFETs increased as drain current was decreased. This effect was attributed to an increase in surface potential roughness at low electron concentrations, where the charge screening effects of electrons become

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\*Private Communication with Roe Maier of AFWL.

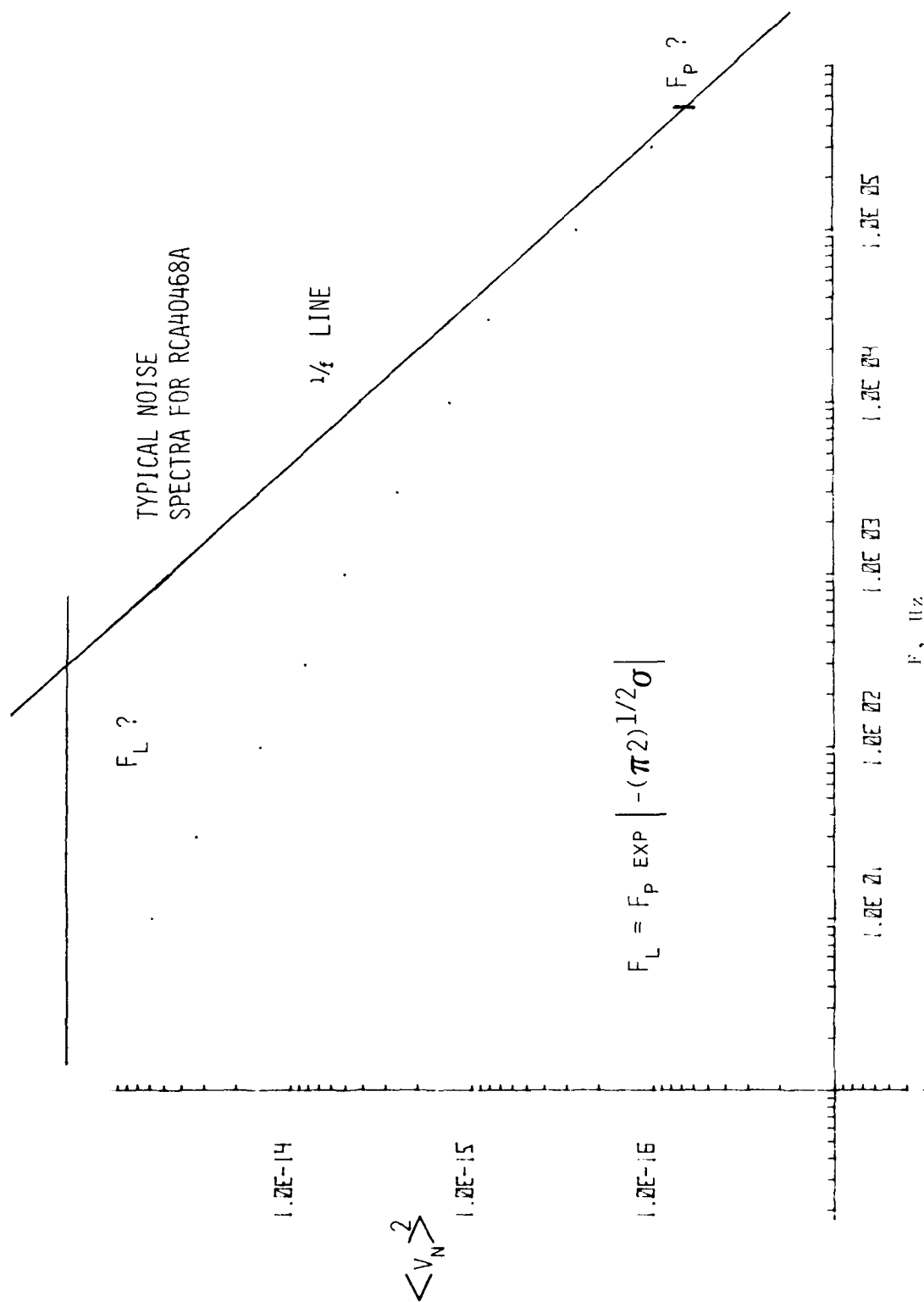


Figure 13. Typical Noise Spectra For RCA 40468A  
 $I_D = 100 \mu A$   $V_D = 5 V$

important. This explanation is remarkably similar to Fowler's (ref. 17) explanation of the low temperature substrate bias effect which Pepper related to hardness. Fowler concludes that "the fluctuations are much more effectively screened than expected as the electrons are forced to the surface." The increase in noise at low drain currents may be a room temperature substitute for the low temperature substrate bias effect. Such measurements would be perfectly suited for the 4470A.

#### 8. CONCLUSION

In conclusion, the HP4470A is not capable of producing data for the evaluation of the standard deviation of surface potential as a total dose screen. However, other methods of analyzing oxide charge show promise and should be explored.

## SECTION VII

### INPUT CURRENT OF INTEGRATED AMPLIFIERS

#### 1. OBJECTIVE

The objective of this experiment was to provide additional support to the observation that input bias current is related to the hardness of linear amplifiers.

#### 2. RATIONALE

The change in offset voltage is the most important total dose effect in linear bipolar amplifiers. Because of the gain in successive circuit stages, it is reasonable to assume that the change in offset voltage in the first stage will dominate the overall response. Therefore, the relative emitter current levels in the input transistors should be a indicator of how much offset voltage change will occur in the amplifier.

#### 3. JUSTIFICATION

The input transistor operating current is the basis for a screen which has been implemented by JPL (ref. 18) and NRL (ref. 19) on LM108 operational amplifiers. The original idea of input current as a screen was developed by Johnston and Skavland (ref. 20), who used input current as a neutron effects screen.

#### 4. PROCEDURE

The offset voltage of test samples was determined along with the necessary information to determine emitter current. The devices were then irradiated and the offset voltage remeasured. The change in offset voltage was then correlated with the average emitter current of the input stage.

## 5. SAMPLES

Twenty-five Fairchild  $\mu$ A741HC operational amplifiers and 25 TI  $\mu$ A733CN video amplifiers were obtained as test samples. The equivalent circuit of the 741 is shown in Figure 14 and the equivalent circuit of the 733 is shown in Figure 15.

## 6. ELECTRICAL TESTS

Offset voltage of the samples was measured using a Tektronix 577 curve tracer with a Tektronix 178 Linear IC Test Fixture. A difference amplifier was required at the outputs of the 733 to enable the offset voltage measurement to be made. Care was taken to ensure that the difference amplifier did not contribute to the offset voltage measured. The gain select nodes of the 733 were biased to yield a gain of 100. Plus and minus supply voltages of the 741 were 15V. Supply voltages of the 733 were plus and minus 6 volts.

To obtain input operating current, the output voltage of the op amp was adjusted to 0 volts and the voltage at the offset null nodes recorded. The amplifier was then removed from the test fixture and the impedance between the offset null and V- was recorded, with the positive lead of the ohmmeter connected to the offset null pin. The current through  $R_1$  and  $R_2$  of Figure 14 can be calculated as the offset null voltage divided by the measured value of  $R_1$  or  $R_2$ , depending on which side was tested. From circuit analysis theory, it can be seen that the current through  $R_1$  and  $R_2$  is approximately equal to the emitter current of  $Q_1$  and  $Q_2$ , respectively. The average emitter current is then calculated as the input operating current.

Similar techniques were used to calculate the input operating current of the 733. Measurements were made between  $G_1$  and  $G_2$  as shown in Figure 15.

EQUIVALENT CIRCUIT

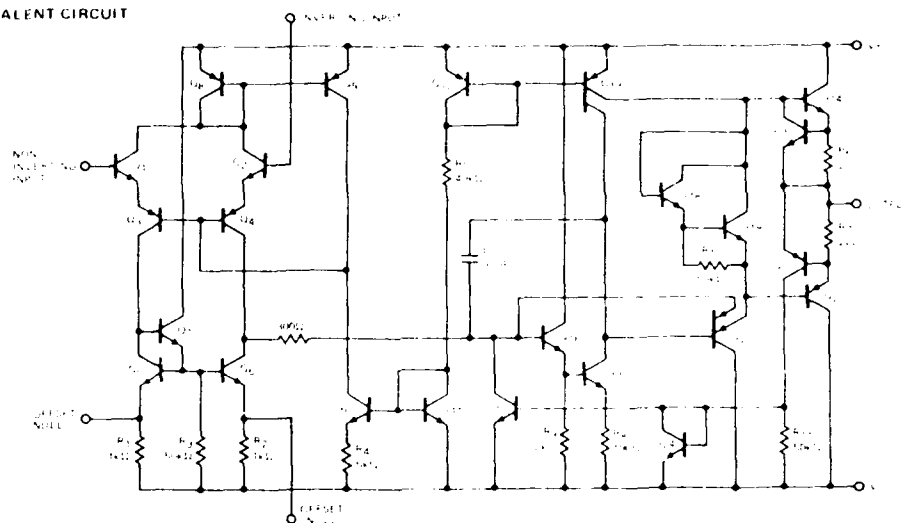
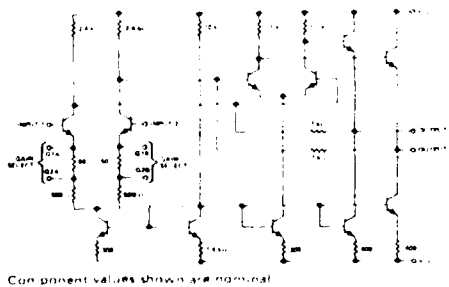


Figure 14. Equivalent Circuit of the 741 Operational Amplifier



Component values shown are nominal

Figure 15. Equivalent Circuit of the 733 Video Amplifier

## 7. RESULTS

The average input operating current for the 25 741's was 6.85 nA with a standard deviation of 9.82. The average input operating current for the 733's were 1.85 mA with a standard deviation of 0.029. Because the standard deviation of the input operating current is small compared to the expected deviation in offset voltage changes, the 733's were dropped from the experiment.

## 8. IRRADIATION

The test devices remaining were irradiated by exposure to the AFWL 5 kilocurie  $\text{Co}^{60}$  gamma ray source. The devices were irradiated to a total ionizing dose of  $1 \times 10^6$  Rad (Si). During the irradiation, the devices were configured as unity gain amplifiers as shown in Figure 16.

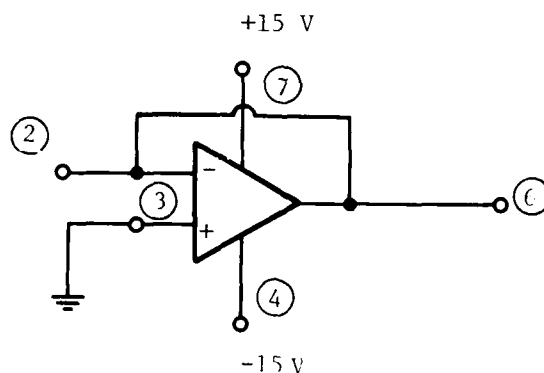


Figure 16. Irradiation Bias Configuration

## 9. RESULTS

A plot of the change in offset voltage as a function of the input operating current is shown in Figure 17. A least squares fit to the data is also shown.

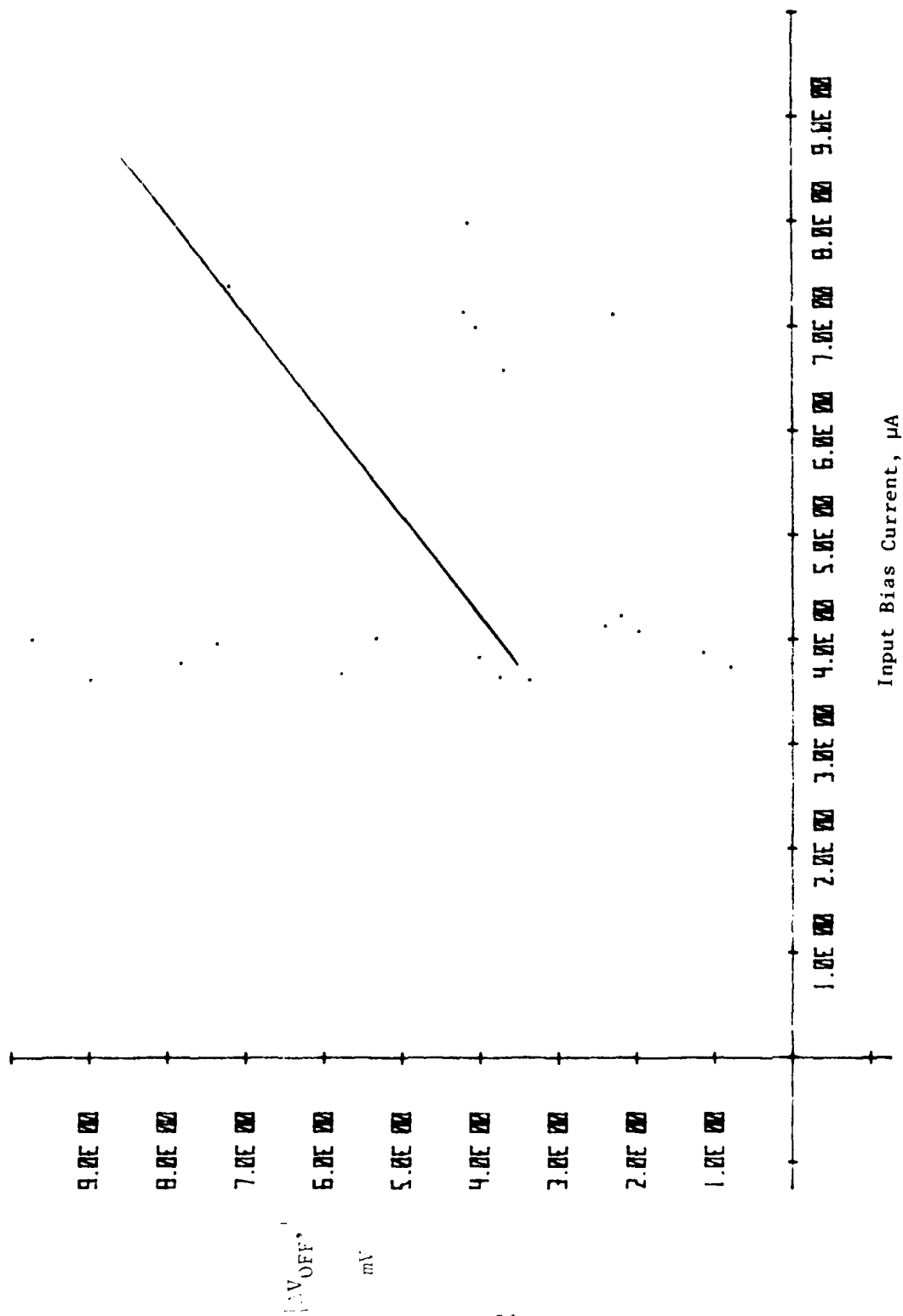


Figure 17. Change in Offset Voltage as a Function of the Average Input Bias Current.  $R = 0.59 \pm 0.14$

The positive slope of the fitted line and the poor correlation coefficient indicate that input operating current was not an indicator of total dose hardness for this set of experimental conditions.

#### 10. CONCLUSIONS

The results obtained in this experiment do not conclusively prove or disprove the hypothesis that input bias currents may be used as a screen for operational amplifiers. JPL used input bias current as a diffusion lot screen and not as a discrete parts screen. The data of Figure 17 suggests that test devices were from two diffusion lots. Therefore, only two data points are available to determine if input bias could be a lot screen for 741 operational amplifiers. Two data points are insufficient to determine the validity of the technique as a lot screen. As a part level screen it certainly appears invalid for the mA741. However, the test vehicle chosen for the phase II tests will allow the input operating current to be varied over a wide range such that the spread in  $\Delta 1/\beta$  of the input transistor can be determined at several different current levels and compared to the spread in average  $\Delta 1/\beta$  between the current levels. This will indicate how well the technique will work as a function of the maximum spread in input operating current.

## SECTION VIII

### IRRADIATE AND ANNEAL

#### 1. OBJECTIVE

The objective of this experiment was to verify that annealing reduces total dose damage to an acceptable level and that an equivalent reirradiation exposure will produce a comparable level of damage.

Irradiate and Anneal (IRAN) is a 100 percent screen applicable to any silicon technology device. The devices are exposed to the expected threat level dose under worst case bias conditions and any devices not meeting the threat level are rejected. The remaining devices are annealed and used in the system.

#### 2. JUSTIFICATION

IRAN has been studied by several investigators (refs. 21, 22, 23, 24, and 25). Mixed results have been obtained for the wide range of techniques tried. For IRAN to be implemented as a screen, it must possess two features. First, it must be verified that enough damage can be annealed out to allow the device to pass its electrical specifications and not degrade the failure rate. Secondly, it must be demonstrated that upon reirradiation, the level of damage at the same dose as the original irradiation will produce a comparable amount of damage.

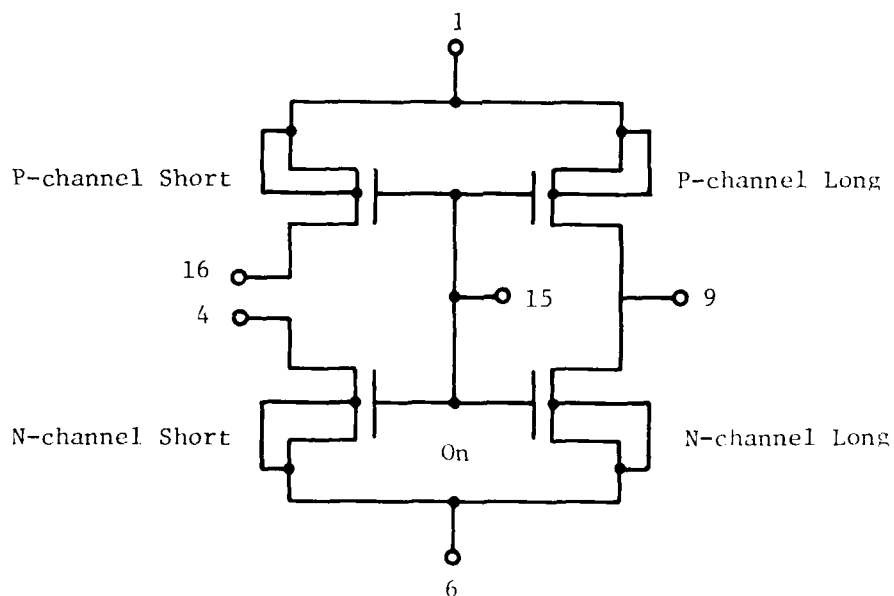
#### 3. PROCEDURE

The test devices in this experiment were split into three groups. The groups were irradiated at  $1 \times 10^5$ ,  $5 \times 10^5$ , and  $1 \times 10^6$  Rad (Si) by Harris Semiconductor. The devices were then annealed. Many annealing times and temperatures have been tried by various investigators with wide results. An anneal bake at 300°C for 6 hours was chosen. The devices were then reirradiated under the same conditions as the first irradiation.

#### 4. SAMPLES

The test samples used were 26 special test structures supplied by Harris Semiconductor. Figure 18 is a circuit diagram of the four MOS transistors. The structure consists of two N-channel and two P-channel devices. One of the N/P channel devices has a short channel while the other has a long channel. The devices were manufactured using hard and soft processes.

Circuit:



Bias for Irradiations: +10 Volts to pins 1 and 15  
0 Volts to pin 6  
Short pin 4 to pin 16

Figure 18. Harris Semiconductor Special MOSFET Test Structure

## 5. ELECTRICAL TESTS

The threshold voltage of each device on every unit was determined by measuring the gate voltage at which the drain current equaled  $1\mu\text{A}$ . The drain voltage was set equal to the gate voltage. Harris Semiconductor made the threshold voltage measurements before and after the first irradiation.

## 6. IRRADIATION

The first irradiations were conducted by Harris Semiconductor. The second irradiations were conducted by BDM using the AFWL 5 kilocurie  $\text{Co}^{60}$  source. Three separate irradiations were conducted to duplicate the original levels of  $1 \times 10^5$ ,  $5 \times 10^5$ , and  $1 \times 10^6$  Rad (Si). The bias used for all irradiations is given in Figure 18.

## 7. RESULTS

The statistical results of the experiment are listed in Table 7. The change in threshold voltage produced by the initial irradiation is plotted as a function of the change in threshold voltage produced by the second irradiation in Figures 19a-d. The correlation coefficient and least squares fit line is included on each plot.

The information in Table 7 indicates that a sputter metallization process produces damage very similar to the damage caused by total ionizing dose. Referring to Figure 10, if sputtering produces a damage equivalent to dose  $X_2$ , then any additional irradiation will cause a negative change in the threshold voltage shift. A negative threshold voltage shift is observed for the sputter metallized devices.

The sputter damage phenomenon also explains why the anneal bake was much more successful for the flash metallized parts. The anneal bake removed part of the sputter produced damage.

TABLE 7. IRAN RESULTS

| $\Delta V_T$ |      |           |       |       |           |       |           |       |       | $V_T(\text{Initial})/V_T(\text{Anneal})$ |       |           |       |           |       |           |       |
|--------------|------|-----------|-------|-------|-----------|-------|-----------|-------|-------|--|-------|-----------|-------|-----------|-------|-----------|-------|
| Flash        |      |           |       |       | Sputter   |       |           |       |       | Flash                                    |       |           |       | Sputter   |       |           |       |
| N-Channel    |      | P-Channel |       |       | N-Channel |       | P-Channel |       |       | N-Channel                                |       | P-Channel |       | N-Channel |       | P-Channel |       |
| Short        | Long | Short     | Long  | Short | Long      | Short | Long      | Short | Long  | Short                                    | Long  | Short     | Long  | Short     | Long  | Short     | Long  |
| N            | 19   | 11        | 25    | 15    | 11        | 6     | 11        | 6     | 11    | 6  | 25    | 24        | 25    | 24        | 11    | 11        | 11    |
| $\bar{X}$    | 0.60 | 0.65      | -0.28 | -0.32 | -0.97     | -1.91 | -2.23     | -2.96 | 0.91  | 0.92                                     | 0.97  | 0.97      | 0.97  | 0.76      | 0.76  | 1.14      | 1.15  |
| $\sigma$     | 0.32 | 0.34      | 0.12  | 0.14  | 1.16      | 1.33  | 1.16      | 1.28  | 0.039 | 0.041                                    | 0.023 | 0.023     | 0.083 | 0.082     | 0.039 | 0.037     | 0.037 |
| Max          | 1.25 | 1.25      | -0.15 | -0.15 | 0.50      | 0.45  | -0.70     | -0.80 | 0.97  | 1.01                                     | 1.01  | 1.01      | 1.00  | 0.87      | 0.87  | 1.23      | 1.22  |
| Min          | 0.20 | 0.25      | -0.55 | -0.60 | -2.50     | -2.95 | -3.75     | -3.95 | 0.82  | 0.082                                    | 0.93  | 0.93      | 0.93  | 0.65      | 0.67  | 1.10      | 1.10  |

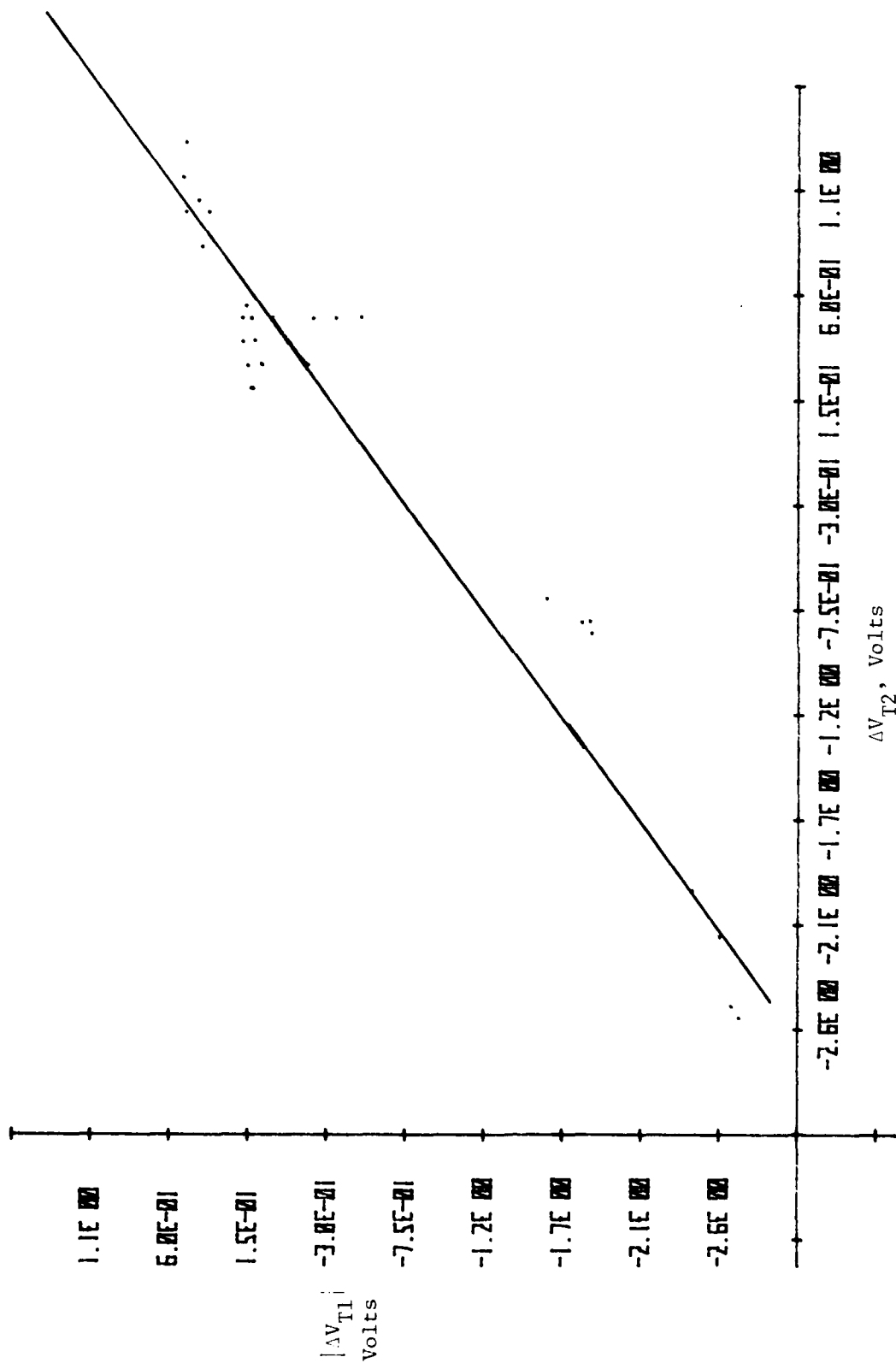


Figure 19a. Comparison of Damage Produced Between First and Second Irradiation. Short N-Channel Devices.  $R = 0.96$

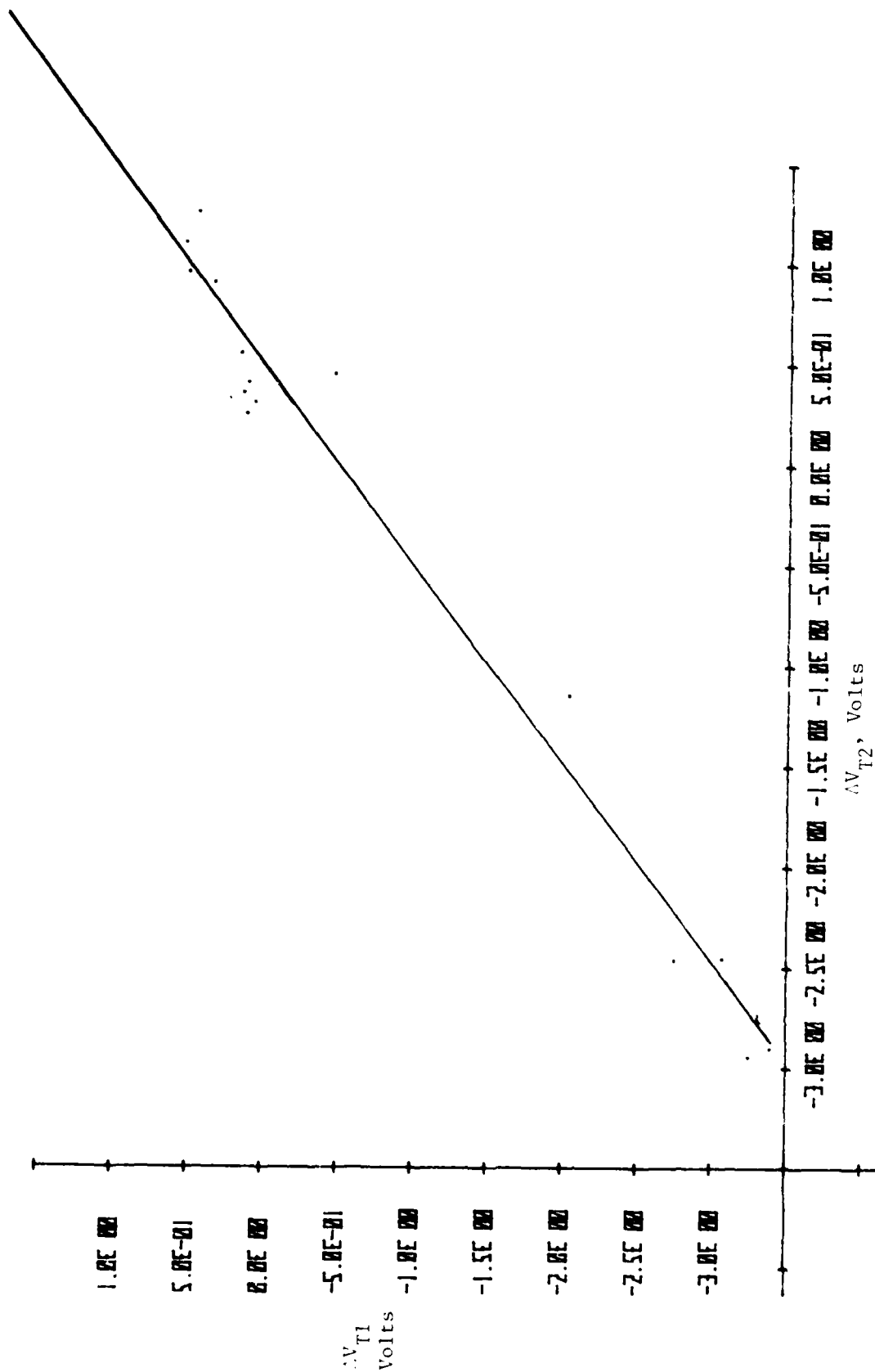


Figure 19b. Comparison of Damage Produced Between First and Second Irradiation. Long N-Channel Devices.  $R = 0.987$

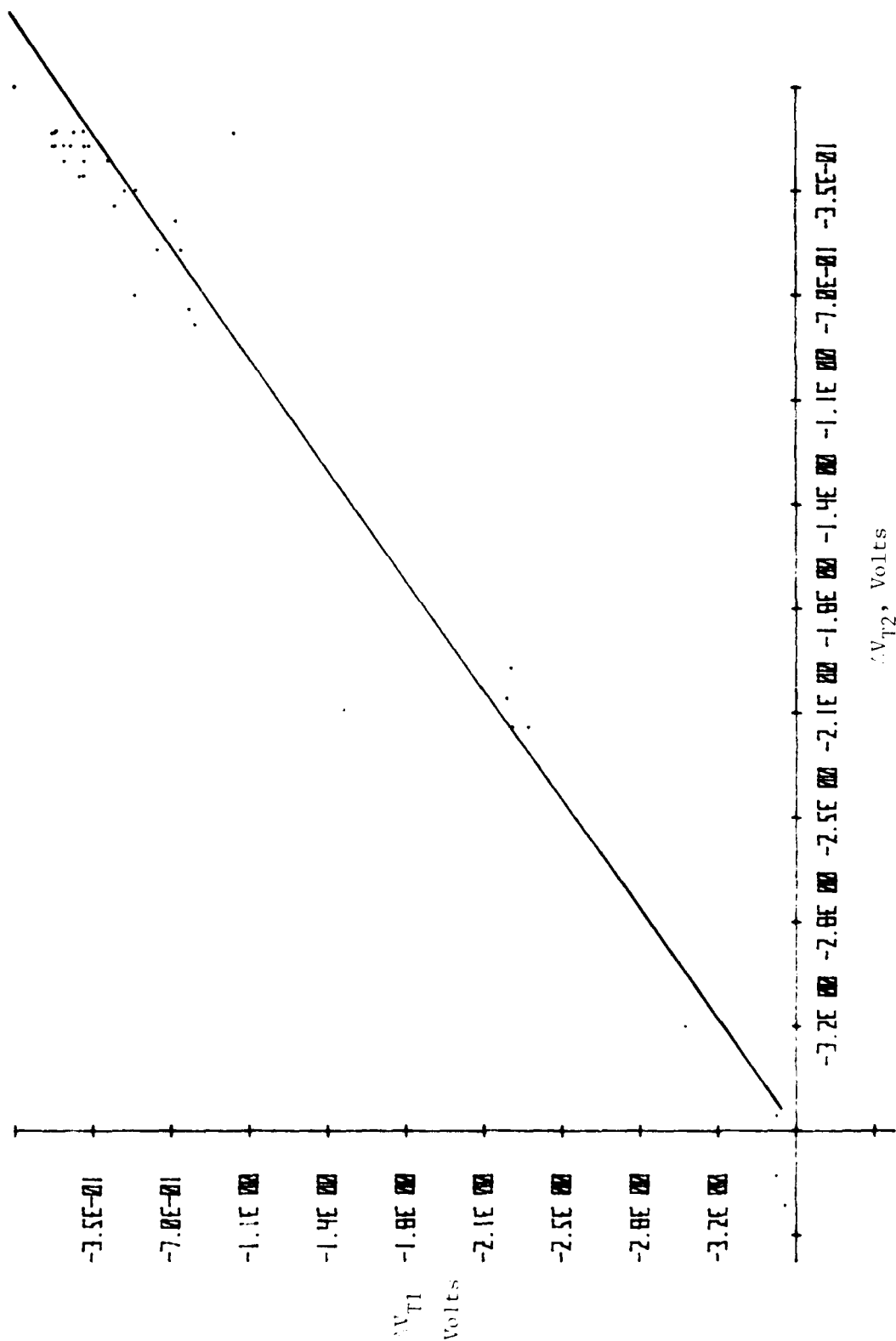


Figure 19c. Comparison of Damage Produced Between First and Second Irradiation. Short P-Channel Devices.  $R = 0.987$

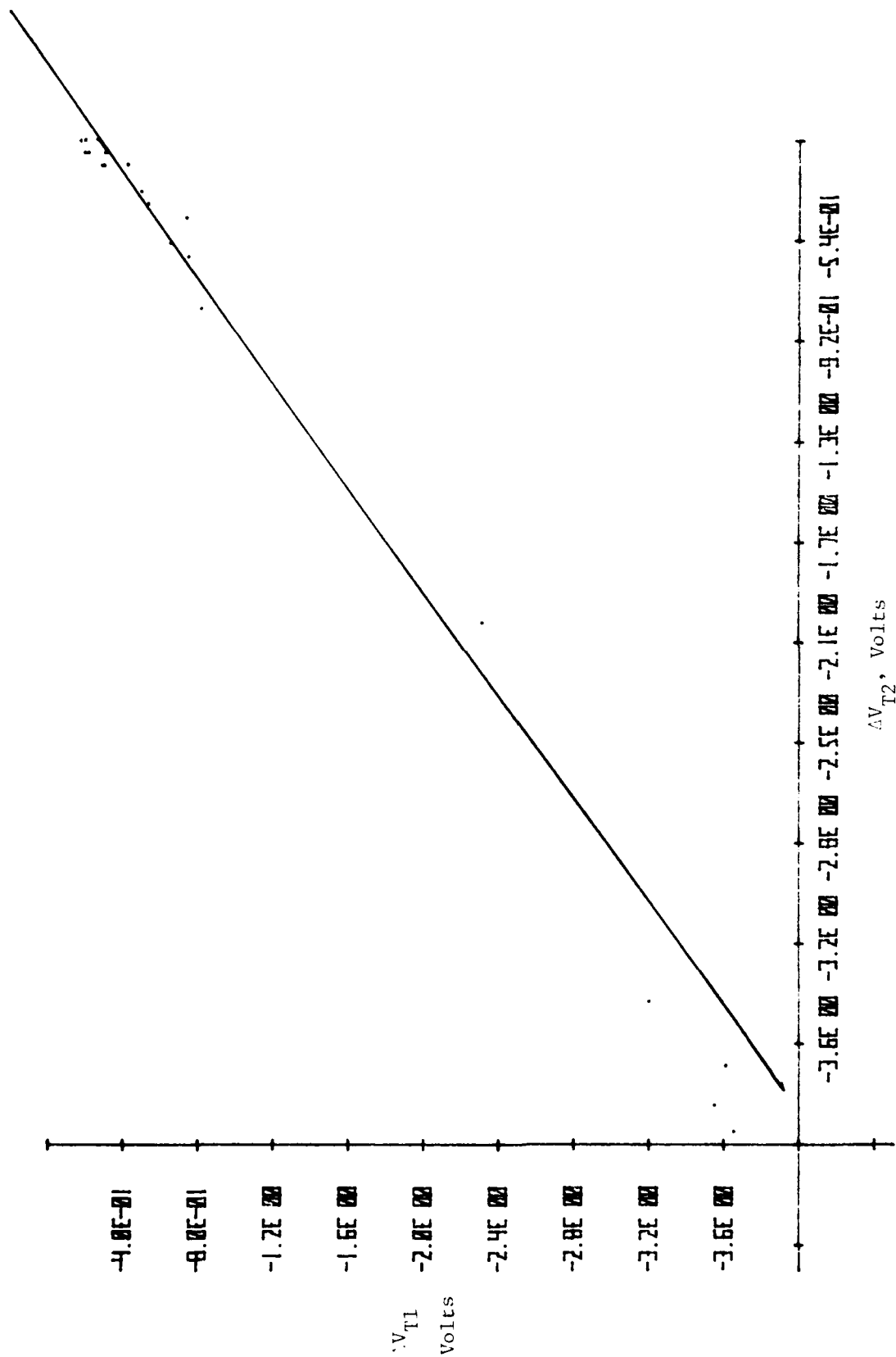


Figure 19d. Comparison of Damage Produced Between First and Second Irradiation. Long P-Channel Devices.  $R = 0.996$

The results of Table 7 indicate that annealing is much more successful on P-channel devices than on N-channel structures. The reason for this effect is not clear.

The results of Figures 19a-d show a good correlation between the threshold voltage shift produced by the first and second irradiation. The correlation suggests that radiation damage is reproducible after an anneal bake.

A disturbing feature of Figures 19a-d is the good fit shown by the sputtered devices. If the anneal had been completely successful, the sputtered parts should have shown the positive threshold voltage shift experienced by the flash metallized parts. An explanation for this effect has not yet been developed.

#### 8. CONCLUSION

The overall results obtained in this IRAN experiment support the use of IRAN as a total dose screen, if the annealing is performed at a sufficiently high temperature.

## SECTION IX

### SUMMARY AND CONCLUSIONS

A summary of the results obtained in the phase I verification testing is given in Table 8. The technique is listed along with the parameters which were correlated and the results of the correlation. The test vehicle and sample size are also given.

The most positive results obtained were for the IRAN tests on the discrete MOS devices. Although these preliminary verification tests (except for IRAN) were inconclusive, they provided much insight for future tests. It is now believed that E-B avalanche tests should be performed on gated devices in order to control hole injection into the oxide. It became obvious that in order for the input operating current to be sensitive to the radiation induced shift in offset voltage, there must be a large variation in the operating current from device to device or lot to lot.

An approach other than the one selected in these tests will have to be taken in order to measure the room temperature effects of dipoles at the interface. BDM is currently investigating the use of conductance versus frequency curves.

The results that were particularly disappointing were those for the hole injection techniques. It was hoped that various "stress" tests could be used to simulate the effects of ionizing radiation by causing hole trapping and interface state generation. Part of the problem with the results obtained may have been due to the test vehicle chosen. It was discovered, after the tests had been performed, that the 40468A is a DMOS device. Although this should not invalidate the results, the structure presents additional variations from a conventional MOSFET which could make the data interpretation more difficult.

In addition to the nonconventional structure used for the stress tests, the approach taken was too simplistic. It is well known that damage as a function of dose is nonlinear and saturates at some level. The "growth curves" for stress have not been characterized but they

TABLE 8. SUMMARY OF PHASE I VERIFICATION TEST RESULTS

| TECHNIQUE                                     | TEST VEHICLE  | SAMPLE SIZE          | PARAMETERS CORRELATED   | CORRELATION COEFFICIENT  |
|---|---|----------------------|---|--|
| 1. Avalanche hole injection                   | RCA 40468A  | 10                   | $\Delta V_G(\text{stress}) : \Delta V_T(\gamma)$<br>[for constant BV]   | $-0.355 \pm 0.31$  |
| 2. Negative bias temperature stress           | 40468A MOSFET   | 7                    | $\Delta V_T(\text{stress}) : \Delta V_T(\gamma)$  | $0.83 \pm 0.14$  |
|   |   | 15                   | $\Delta V_T(\text{stress}) : \Delta V_T(\gamma)$<br>$\Delta n(\text{stress}) : \Delta n(\gamma)$  | $-0.304 \pm 0.25$<br>$-0.121 \pm 0.27$                                     |
| 3. E-B avalanche on bipolar transistors       | 2N3468 PNP, power<br>2N2720 NPN, low power<br>2N2944 PNP, low power<br>2N2537 NPN, switch | 10<br>10<br>10<br>10 | $\Delta I/\beta(\text{stress}) : \Delta I/\beta(\gamma)$<br>$\Delta I/\beta(\text{stress}) : \Delta I/\beta(\gamma)$<br>$\Delta I/\beta(\text{stress}) : \Delta I/\beta(\gamma)$<br>$\Delta I/\beta(\text{stress}) : \Delta I/\beta(\gamma)$              | $-0.11 \pm 0.35$<br>$0.64 \pm 0.21$<br>$0.62 \pm 0.22$<br>$-0.64 \pm 0.21$ |
| 4. Edge states by low frequency noise         | 40468A MOSFET   | 10                   | $e_n^2(10\text{Hz}) : \Delta V_T(\gamma)$   | $-0.22 \pm 0.34$   |
| 5. Dipole density from noise versus frequency | 40468A MOSFET   |                      | No results (could not measure $\sigma$ from $e_n^2$ versus frequency)   |  |
| 6. Input operating of linear circuits         | A741 op amp.<br>A733 video amp.   | 25<br>25             | $I_1 : \Delta V_{\text{off}}(\gamma)$<br>No results (spread in $I_1$ too small)   | $0.59 \pm 0.14$  |
| 7. IRAN                                       | Special P and N-Channel test Transistors from Harris Semiconductor                        |                      | N-Channel $\Delta V_T(\gamma_1) : \Delta V_T(\gamma_2)$ short<br>N-Channel $\Delta V_T(\gamma_1) : \Delta V_T(\gamma_2)$ long<br>P-Channel $\Delta V_T(\gamma_1) : \Delta V_T(\gamma_2)$ short<br>P-Channel $\Delta V_T(\gamma_1) : \Delta V_T(\gamma_2)$ | 0.960<br>0.987<br>0.987<br>0.996   |

are assumed also to be nonlinear. A more thorough approach to the verification of the stress test technique would involve a complete characterization of the parameter shift versus stress curve at several different electric field strengths. These could then be compared to the  $\Delta V_T$  versus dose curves in order to identify similarities in slope and to best select an appropriate stress and dose level to determine correlation.

In conclusion, the phase I verification tests have provided valuable information on how to conduct the phase II verification tests, even though these preliminary results were not encouraging.

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The following bibliography is a list of the articles obtained and reviewed for this program listed in alphabetical order by author. Two additional sources were not included in this bibliography because of the sheer volume of relevant articles. Several hundred articles pertinent to semiconductor total dose response, hardening, and hardness assurance, are published in the IEEE Transactions on Nuclear Science No. 6 published each December. This issue contains selected papers presented at the annual IEEE Conference on Nuclear and Space Radiation Effects. This conference was started in 1964 with conference papers being published in the November issue for 1964 and the October issue in 1965. From 1966 the conference papers have appeared in the December issue. A recent publication which contains numerous articles of interest for total dose phenomena in semiconductors is the Proceedings of the International Topical Conference on the Physics of  $\text{SiO}_2$  and Its Interfaces. The papers presented at this conference have been published in book form by Pergamon Press titled The Physics of  $\text{SiO}_2$  and Its Interfaces, editor Sokrates T. Pantelides, 1978, Pergamon Press., Inc.

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